

LIBRARY OF THE
UNIVERSITY OF ILLINOIS
AT URBANA-CHAMPAIGN

510.84

I l 6 r

no. 160-170

cop. **2**



The person charging this material is responsible for its return to the library from which it was withdrawn on or before the **Latest Date** stamped below.

Theft, mutilation, and underlining of books are reasons for disciplinary action and may result in dismissal from the University.

UNIVERSITY OF ILLINOIS LIBRARY AT URBANA-CHAMPAIGN

NOV 15 1973

NOV 15 1973



Digitized by the Internet Archive
in 2013

<http://archive.org/details/incrementalcharg166nusp>

r
66
3

DIGITAL COMPUTER LABORATORY

UNIVERSITY OF ILLINOIS

URBANA, ILLINOIS

REPORT NO. 166

AN INCREMENTAL CHARGE METHOD FOR THE ANALYSIS OF NONLINEAR CIRCUITS

by

Stephen John Nuspl

August 6, 1964

This work is being submitted in partial fulfillment of the requirements for the Degree of Master of Science, August, 1964, and was supported in part by the Office of Naval Research under contract Nonr-1834(15).)

DIGITAL COMPUTER LABORATORY
UNIVERSITY OF ILLINOIS
URBANA, ILLINOIS

REPORT NO. 166

AN INCREMENTAL CHARGE METHOD FOR THE ANALYSIS OF NONLINEAR CIRCUITS

by

Stephen John Nuspl

August 6, 1964

This work is being submitted in partial fulfillment of the requirements for the Degree of Master of Science, August, 1964, and was supported in part by the Office of Naval Research under contract Nonr-1834(15).)

ACKNOWLEDGMENTS

The author would like to express his sincerest thanks to his advisor, Professor W. J. Poppelbaum, for his good counsel, support and encouragement. Thanks are also extended to the past and present Task 15 group at the Digital Computer Laboratory with whom the ideas in this thesis were often discussed and to Mrs. Phyllis Olson who prepared the final manuscript. The excellent drawings in this report are a result of the good work of the Digital Computer Laboratory Drafting Department under Kenneth Law.

TABLE OF CONTENTS

	Page
1. INTRODUCTION	1
2. DEVELOPMENT OF THE INCREMENTAL CHARGE METHOD	3
2.1 Circuit Ordering and Topological Restrictions	3
2.2 The Charge Distribution Criterion	5
2.3 Node Voltage Calculation	12
3. CALCULATION OF IMPEDANCE FACTORS	15
4. VOLTAGE-CONTROLLED SUBNODES	20
5. DISCUSSION OF CORRECTION FORMULA	26
5.1 Error Term for a Branch	26
5.2 Compensation of the Error	28
5.3 A Predictor-Corrector Type Method	30
6. ERRORS AND STABILITY	33
6.1 Circuit Error and Response Error	33
6.2 Stability	35
7. RELAXATION OF TOPOLOGICAL RESTRICTIONS	37
8. NONLINEAR AND TIME-VARYING PARAMETERS	40
8.1 Sources	40
8.2 Nonlinear Elements	40
8.3 Semiconductor Diodes	41
8.4 Transistors	45
8.5 Transmission Lines	53
9. REALIZATION OF THE IQ METHOD	58
9.1 The Program	58
9.2 Sample Results	60
9.3 Efficiency	61
10. CONCLUSIONS	63
BIBLIOGRAPHY	65
APPENDIX	66

AN INCREMENTAL CHARGE METHOD FOR THE ANALYSIS OF NONLINEAR CIRCUITS

Stephen John Nuspl, M.S.

Department of Electrical Engineering

University of Illinois, 1964

Conventional numerical methods for nonlinear transient circuit analysis apply standard numerical procedures to the equations obtained from Kirchhoff's laws. In this thesis is developed a method of analysis in which only one of Kirchhoff's laws is forced to hold and the other is used to make numerical corrections. The method developed here assumes that the current law holds and the voltage law may be violated.

To obtain sufficiently simple numerical formulas, a circuit with a tree-type topology is assumed. Relying on this the basic charge distribution and node voltage calculation formulas are derived for the general branch which may consist of a resistance, a capacitance, an inductance, a voltage source or any series combination of these. Since this method favors current controlled nonlinear elements, an analogous but more restricted method for conveniently including voltage-controlled devices is developed. A brief discussion of errors and their compensation and of stability is included.

Because of the importance of diodes and transistors, the technique by which they can be efficiently analyzed by the method is developed. The advantages are that the method provides for the models the means for making numerical corrections. A technique by which transmission lines can be handled is also described.

A program based on this method is presented through a brief description. To illustrate the use of the method four sample circuits and the waveforms they produced are given. It is concluded that the method has some decided advantages which should prove to make it useful, but not enough experience has been had with it to make any meaningful comparison with other efficient methods for nonlinear circuit analysis.

1. INTRODUCTION

In the analysis of transients in nonlinear circuits one usually attempts to obtain a first-order solution by the use of a linear transform method which relies on a piecewise linear approximation of the nonlinear elements. When this is no longer accurate enough or leads to cumbersome algebraic manipulations, a more basic approach must be used. This normally consists in the writing of the differential equations of the circuit obtained from Kirchhoff's laws and manipulating these until a set of first-order linear equations in the form

$$\left[\dot{x}_k \right]_{m,l} = \left[a_{ki} \right]_{m,n} \left[x_i \right]_{n,l}$$

is obtained. a_{ki} is either a constant or a variable depending on any x_i . For any but the simplest of circuits a numerical integration must be used. This method has a number of disadvantages which become more and more severe as the size of the circuit increases: finding the coefficients a_{ki} is usually a time-consuming job; the evaluation of the coefficients at each step requires considerable computer time since the coefficients in general contain some terms related to the nonlinear elements; the addition of only one more element in the circuit might require that new expressions for all coefficients be found and programmed. These inconveniences severely restrict the practical use of this technique for the solution of transients in larger nonlinear networks.

Mechanizations of the above method which essentially separate the linear elements from the nonlinear are found in the literature.^[1,3] The linear part of the circuit is usually described by a coefficient matrix which is automatically assembled and inverted by program. The linear and nonlinear portions are then integrated separately and matched at convenient time intervals. This class of methods is excellent in that only a description of the circuit topology

and elements must be supplied. However, considerable programming effort is required to make the methods functional and sometimes there are stability problems.

The Incremental Charge (IQ) method described in this thesis in essence goes back one step to more basic principles. In all of the above methods it was assumed that Kirchhoff's current and voltage laws hold and from these the differential equations were obtained. In the Incremental Charge method we impose one of Kirchhoff's laws, allow the other to be temporarily relaxed and use the deviations from this law as a means of making numerical corrections. The process must always tend towards the reduction of the deviations. Programs for the dc analysis of circuits by the use of these principles have been successfully used^[5,7] but the extension of these principles into the time domain does not yet seem to have been attempted.

2. DEVELOPMENT OF THE INCREMENTAL CHARGE METHOD

The basic philosophy behind the IQ method is that one of Kirchhoff's laws will be allowed to be violated in order to permit numerical incremental corrections. We can allow either the voltage around a circuit loop to be in error by a small amount or we can relax the requirement that the algebraic sum of the currents flowing into a node be zero. It was found that allowing Kirchhoff's voltage law (KVL) to be violated and strictly enforcing Kirchhoff's current law (KCL) seemed to result in a more convenient formalization of a numerical procedure. It is therefore this principle on which the IQ method is based.

2.1 Circuit Ordering and Topological Restrictions

The first task is to devise a convenient scheme for presenting the circuit topology to the computer and an order among the circuit elements which the program follows during the execution of the method. To accomplish this each node of the circuit will be assigned a number which is also defined as the "level" of that node. This notion of levels of nodes is introduced here only for the reason that it conveys better the concept of ordering among the nodes than the word "number." The reference node is always assigned the number 1. These definitions are illustrated in Fig. 2.1. Between any two nodes there can be branches which may consist of a capacitance, a resistance, an inductance, a voltage source or any combination of these. These branches also have numbers assigned to them but since only the knowledge of which ones are under a particular node is required, the ordering can be arbitrary.

To define a sufficiently simple numerical procedure a number of restrictions will be placed on the circuit topology. First it will be assumed that the topology is in the form of a tree as shown in Fig. 2.1. The forcing

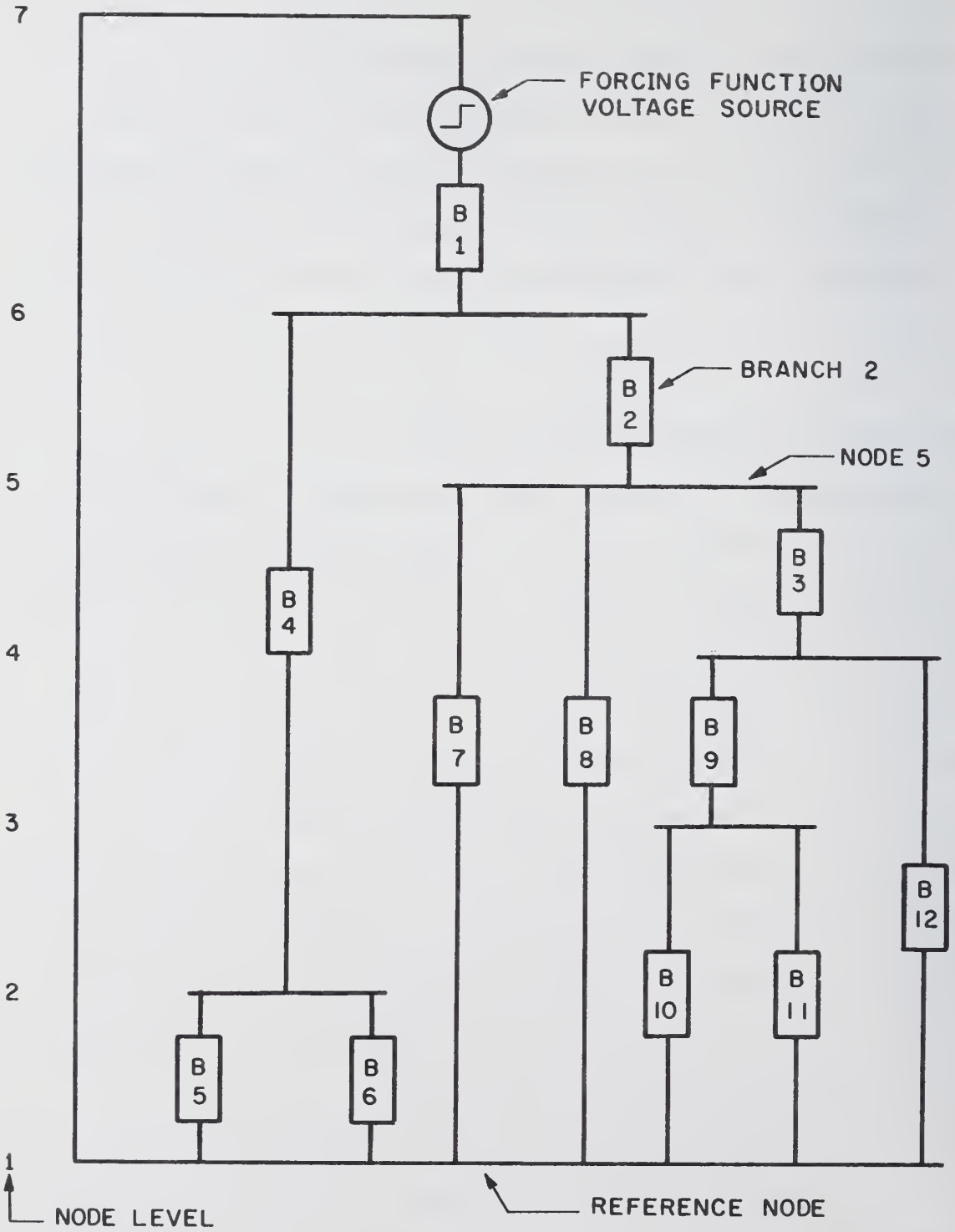


Figure 2.1. Assumed Form of Topology for Development of Method.

function to which the circuit must respond is in the branch at the apex of the diagram and in the form of a voltage source. The second restriction is that there be at most one branch between two nodes of which the reference node is not one. These restrictions may seem drastic at present, but many nonlinear circuit problems fall directly into this type of topology and many others which do not conform to these assumptions can be handled but the error will be slightly larger and other conveniences of the method are forfeited. The second restriction will eventually be eliminated entirely and the relaxation of the first will be discussed later.

2.2 The Charge Distribution Criterion

There are essentially two steps in the numerical procedure. In the first a current is injected into the highest node and passed to successively lower level nodes via the branches under each. When the current distribution is completed, the currents in all branches are known, enabling us to calculate the voltage across each element. The second step then consists in starting from the reference node and determining what each successively higher level node voltage will be.

To develop this method, let us consider the general node of Fig. 2.2 which is assumed to have n branches immediately below it. In a time interval Δt_i a current I_{ki} or, equivalently, a charge

$$\Delta Q_{ki} = I_{ki} \Delta t_i$$

is injected into node k from higher level nodes. By a distribution process which is to be developed branch j receives an amount of charge ΔQ_{ji} . The assumption that KCL holds implies that

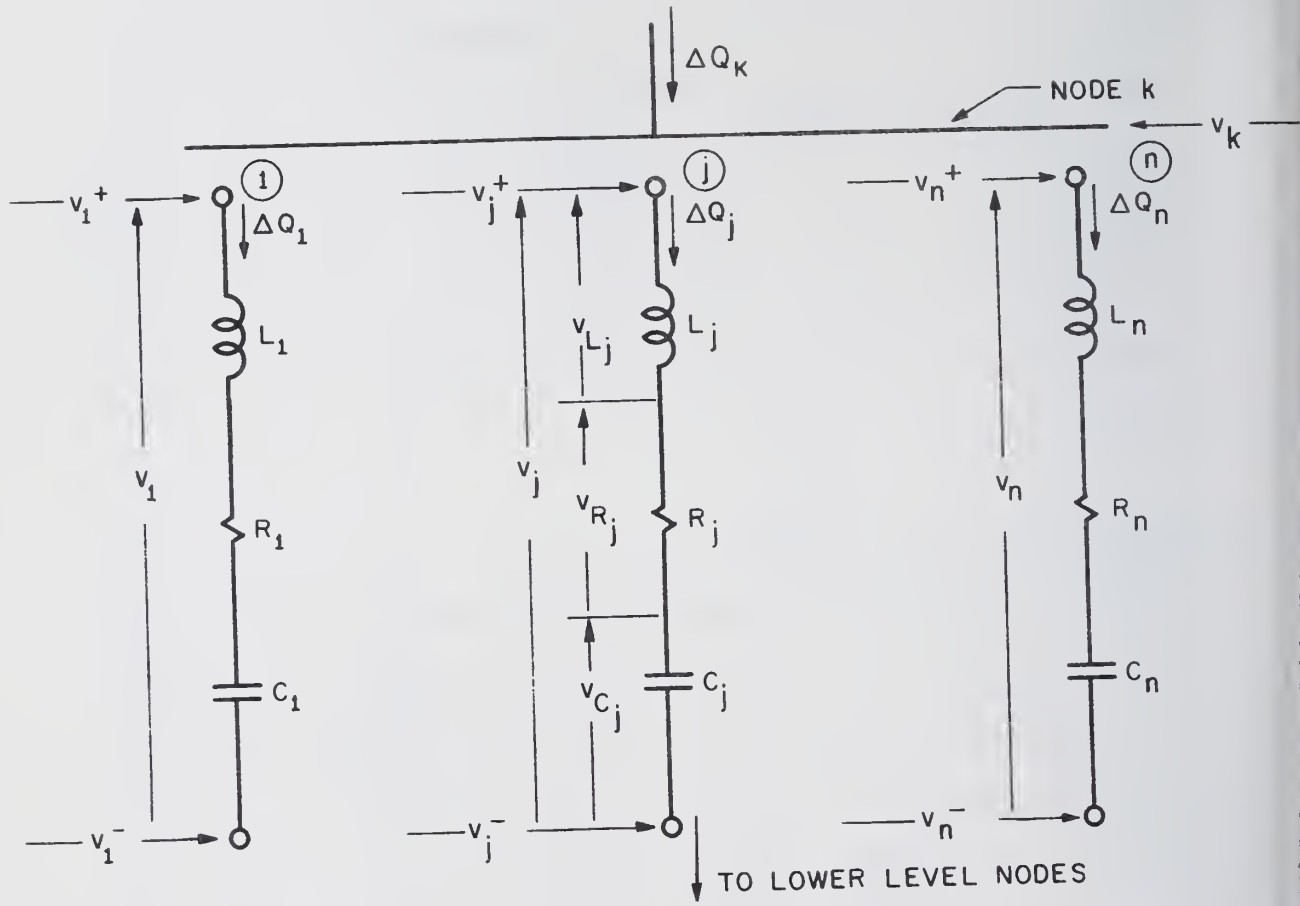


Figure 2.2. The General Node.

$$\Delta Q_{ki} = \sum_{j=1}^n \Delta Q_{ji} \quad (2.1)$$

The branches in Fig. 2.2 are not shown connected to node k to emphasize that voltage v_k and all v_{ji}^+ 's may have different values if KVL does not hold. If we required that it does hold, we have

$$v_{ki} = v_{li}^+ = v_{2i}^+ = \dots = v_{ni}^+ \quad (2.2)$$

since the points (1) to (n) at the branch tops are connected to node k in the actual circuit. If we permit this last set of equations to be violated, we are allowing voltage differences

$$\Delta v_{ji} = v_{ki} - v_{ji}^+ \quad (2.3)$$

If this Δv_{ji} approaches zero, KVL will again hold. Hence an exact solution of the circuit will be had if this condition holds over the entire network. Therefore, the object of the numerical method will be to keep this voltage difference as small as possible, or at least below a tolerable level.

The problem now is to distribute the charge ΔQ_{ki} among the branches in such a manner that all branch voltages v_j^+ will experience an approximately equal increase. To accomplish this we define a set of differences by

$$\begin{aligned} \Delta Q_{ji} &= Q_{ji} - Q_{j(i-1)} \\ \Delta^2 Q_{ji} &= \Delta Q_{ji} - \Delta Q_{j(i-1)} \\ \Delta^3 Q_{ji} &= \Delta^2 Q_{ji} - \Delta^2 Q_{j(i-1)} \end{aligned} \quad (2.4)$$

The voltages developed across the three types of elements are then given by

$$v_{cji} = \frac{Q_{ji}}{c_j} \quad v_{Rji} = R_j \frac{\Delta Q_{ji}}{\Delta t_i} \quad v_{Lji} = L_j \frac{\Delta^2 Q_{ji}}{(\Delta t_i)^2} \quad (2.5)$$

Since we are allowing each branch to contain all three types of elements, we see that only $\Delta^3 Q_{ji}$ can be changed arbitrarily; the other charge differences must be determined by equations 2.4. Also define

$$\Delta v_{ji}^+ = v_{ji}^+ - v_{j(i-1)}^+ \quad (2.6)$$

We are now in a position to define three series impedance factors between point

(j) of Fig. 2.2 and the reference node:

$$Z_{cj} = \frac{\Delta v_{cEji} \Delta t_i}{\Delta Q_{ji}} \quad (2.7)$$

$$Z_{Rj} = \frac{\Delta v_{REji} \Delta t_i}{\Delta^2 Q_{ji}} \quad (2.8)$$

$$Z_{Lj} = \frac{\Delta v_{LEji} \Delta t_i}{\Delta^3 Q_{ji}} \quad (2.9)$$

where v_{cE} , v_{RE} and v_{LE} are the voltages developed across these series impedance factors and which satisfy the relations

$$v_{ji}^+ = v_{cEji} + v_{REji} + v_{LEji} \quad (2.10)$$

and

$$\Delta v_{ji}^+ = \Delta v_{cEji} + \Delta v_{REji} + \Delta v_{LEji} \quad (2.11)$$

We can also define a total branch impedance factor

$$Z_j = Z_{cj} + Z_{Rj} + Z_{Lj} \quad (2.12)$$

and two admittance factors

$$Y_j = \frac{1}{Z_j} \quad (2.13)$$

$$Y_k = \sum_{j=1}^n Y_j \quad (2.14)$$

These factors serve as a means of predicting branch voltage increases for a given change in ΔQ_j or in one of the higher differences.

Assume that the numerical procedure has been under way for a number of cycles and that after cycle (i-1) is completed there is a residual voltage error $\Delta v_{j(i-1)}$ between node k and branch j. The first task is to raise the branch voltage v_{ji}^+ to the node voltage $v_{k(i-1)}$ by injecting an appropriate amount of charge which we shall define as $\Delta_R Q_{ji}$ into the branch. Assuming that the three impedance factors are known for the branch, this condition requires $\Delta_R^3 Q_{ji}$ be such that

$$\frac{\Delta Q_{j(i-1)} + \Delta^2 Q_{j(i-1)} + \Delta_R^3 Q_{ji}}{\Delta t_i} Z_{cj} + \frac{(\Delta^2 Q_{j(i-1)} + \Delta_R^3 Q_{ji})}{\Delta t_i} Z_{Rj} + \frac{\Delta_R^3 Q_{ji}}{\Delta t_i} Z_{Lj} = \Delta v_{j(i-1)} \quad (2.15)$$

this yields

$$\Delta_R^3 Q_{ji} = \frac{\Delta t_i}{Z_j} \left[\Delta v_{j(i-1)} - Z_{cj} \left(\frac{\Delta Q_{j(i-1)}}{\Delta t_i} \right) - (Z_{cj} + Z_{Rj}) \frac{\Delta^2 Q_{j(i-1)}}{\Delta t_i} \right] \quad (2.16)$$

this is the basic "correction" formula in the method and will be discussed in more detail later. After determining

$$\Delta_R Q_{ji} = \Delta Q_{j(i-1)} + \Delta^2 Q_{j(i-1)} + \Delta_R^3 Q_{ji} \quad (2.17)$$

for every branch and summing, we have distributed an amount of charge

$$\Delta_R Q_{ki} = \sum_{j=1}^n \Delta_R Q_{ji} \quad (2.18)$$

This leaves an additional charge to be distributed:

$$\Delta_A Q_{ki} = \Delta Q_{ki} - \Delta_R Q_{ki} \quad (2.19)$$

Since it is assumed that at this point all branch voltages are at the level $v_{k(i-1)}$, this additional charge must be distributed so that all branch voltages will increase the same amount. If branch j receives an additional $\Delta_A Q_{ji}$ then

$$\begin{aligned} \Delta^3 Q_{ji} &= \Delta_R^3 Q_{ji} + \Delta_A^3 Q_{ji} \\ \Delta^2 Q_{ji} &= \Delta_R^2 Q_{ji} + \Delta_A^2 Q_{ji} \end{aligned} \quad (2.20)$$

$$\Delta Q_{ji} = \Delta_R Q_{ji} + \Delta_A Q_{ji}$$

Since by definition

$$\begin{aligned} \Delta_R^2 Q_{ji} &= \Delta^2 Q_{j(i-1)} + \Delta_R^3 Q_{ji} \\ \Delta_R Q_{ji} &= \Delta Q_{j(i-1)} + \Delta_R^2 Q_{ji} \end{aligned} \quad (2.21)$$

we get the result

$$\Delta_A^3 Q_{ji} = \Delta_A^2 Q_{ji} = \Delta_A Q_{ji} \quad (2.22)$$

The usefulness of this lies in the fact that the additional charge Δ_{Aji}^Q will cause an increase in branch voltage of

$$\Delta_{Aji}^{v+} = Z_{cj} \frac{\Delta_{Aji}^Q}{\Delta t_i} + Z_{Rj} \frac{\Delta_{Aji}^Q}{\Delta t_i} + Z_{Lj} \frac{\Delta_{Aji}^Q}{\Delta t_i} = \frac{\Delta_{Aji}^Q}{\Delta t_i} (Z_{cj} + Z_{Rj} + Z_{Lj}) = \frac{\Delta_{Aji}^Q}{Y_j \Delta t_i} \quad (2.23)$$

or

$$\Delta_{Aji}^Q = Y_j \Delta t_i \Delta_{Aji}^{v+} \quad (2.24)$$

which gives the amount of charge which must be injected into branch j to raise its voltage Δ_{Aji}^{v+} . We want the voltage of all n branches and that of the node to increase the same amount:

$$\Delta_{Aji}^{v+} = \Delta_{Aki}^v = \text{constant for } j = 1 \text{ to } n \quad (2.25)$$

Hence

$$\Delta_{Aki}^Q = \sum_{j=1}^n \Delta_{Aji}^Q = \sum_{j=1}^n Y_j \Delta_{Aji}^{v+} \Delta t_i = \Delta t_i \Delta_{Aki}^v \sum_{j=1}^n Y_j = \Delta t_i \Delta_{Aki}^v Y_k \quad (2.26)$$

Therefore

$$\frac{\Delta_{Aji}^Q}{\Delta_{Aki}^Q} = \frac{Y_j}{Y_k} \quad (2.27)$$

r

$$\Delta_{Aji}^Q = \Delta_{Aki}^Q \times \frac{Y_j}{Y_k} \quad (2.28)$$

This is the desired formula for distributing the charge $\Delta_{A_{ki}} Q_{ki}$ among the branches.

The term

$$Y_k = \frac{\Delta_{A_{ki}} Q_{ki}}{\Delta t_i \Delta_{A_{ki}} v_{ki}}$$

is in the form of an admittance and since the expression contains only terms related to node k, we could define it as the "admittance factor" for node k. A node impedance factor can therefore be defined by

$$Z_k = \frac{1}{Y_k} \quad (2.29)$$

2.3 Node Voltage Calculation

The above criterion is used to channel the charge injected into the top node through all the branches and other nodes and into the reference node. When this is completed, all the branch currents are known and therefore the voltages across them can be calculated. The remaining step is to calculate the node voltages v_{ki} .

Through possible errors in the impedance factors all the branch voltages v_{ji}^+ will not have the same value. Therefore some sort of mean value for v_{ki} must be defined. There are a number of possible ways of determining this mean, the most primitive of which is the average value:

$$v_{ki} = \frac{1}{n} \sum_{j=1}^n v_{ji}^+ \quad (2.30)$$

A second formula may be obtained by imposing the conservation of energy condition at node k, which implies that no energy is lost through the numerical process.

This condition states

$$v_{ki} \Delta Q_{ki} = \sum_{j=1}^n v_{ji}^+ \Delta Q_{ji} \quad (2.31)$$

and hence we have

$$v_{ki} = \sum_{j=1}^n v_{ji}^+ \frac{\Delta Q_{ji}}{\Delta Q_{ki}} \quad (2.32)$$

This is effective when ΔQ_{ki} and all ΔQ_{ji} 's have the same sign. But, if

$$|\Delta Q_{ki}| \ll \sum_{j=1}^n |\Delta Q_{ji}|$$

which occurs if one of the branches under node k contains a dc source, numerical instabilities may result. A modified version of the formula is

$$v_{ki} = \frac{\sum_{j=1}^n v_{ji}^+ |\Delta Q_{ji}|}{\sum_{j=1}^n |\Delta Q_{ji}|} \quad (2.33)$$

When all ΔQ_{ji} 's have the same sign energy is again conserved; otherwise the node voltage will be the average between the branches delivering power and those receiving it.

In a third method the impedance factors defined for the current distribution are used:

$$v_{ki} = \frac{\sum_{j=1}^n Y_j v_{ji}^+}{Y_k} \quad (2.34)$$

This has the effect of latching the node voltage to the branch with the lowest impedance factor and therefore tends to stabilize the node voltage against

numerical oscillations. Because of this stabilizing effect this last criterion for the calculation of the node voltages seems to be the best. However, no detailed analysis comparing the last two methods has yet been made.

3. CALCULATION OF IMPEDANCE FACTORS

In the above discussion the knowledge of the values of Z_c , Z_R and Z_L for each branch was assumed. Since there are three parameters which must be defined, we need three sets of equations for each branch. This makes impossible the redefining of a set of impedances during each step of the analysis. Though this would be desirable, it is not absolutely necessary. The initially defined impedances will never change if all the elements are linear and will be relatively constant over small ranges of voltages even if the elements are non-linear. In the latter case the impedance factors must be redefined when the actual branch voltage changes start to differ appreciably from the ones predicted with this set of impedance factors. If we adhere to the restrictions in the topology previously mentioned there are two methods which can be used to calculate a new set of impedance factors.

Let us assume that we have the condition

$$\Delta Q_{ki} \gg \Delta_R Q_{ki}$$

or

$$\Delta_A Q_{ki} \approx \Delta Q_{ki}$$

Under this assumption it may be recalled that we will have for each branch

$$\Delta_A^3 Q_{ji} = \Delta_A^2 Q_{ji} = \Delta_A Q_{ji}$$

Therefore

$$\frac{\Delta v_{ji}^+ \Delta t_i}{\Delta_A Q_{ji}} = [Z_{Cj} + Z_{Rj} + Z_{Lj}] = Z_j \quad (3.1)$$

After a complete numerical cycle all the terms on the left are known and therefore the impedance factor Z_j can be calculated.

To separate the three impedance factors two more equations are needed. To obtain these we must first define an equivalent incremental capacitance, resistance and inductance which are in series between point (j) and the reference node:

$$C_{Ej} = \frac{\Delta Q_{ji}}{\Delta v_{CEji}} \quad (3.2)$$

$$R_{Ej} = \frac{\Delta v_{REji}}{\frac{\Delta^2 Q_{ji}}{\Delta t_i}} \quad (3.3)$$

$$L_{Ej} = \frac{\Delta v_{LEji}}{\frac{\Delta^3 Q_{ji}}{(\Delta t_i)^2}} \quad (3.4)$$

Combining these with the definition of Z_{Cj} , Z_{Rj} and Z_{Lj} we get

$$Z_{Cj} = \frac{\Delta t_i}{C_{Ej}} \quad (3.5)$$

$$Z_{Rj} = R_{Ej} \quad (3.6)$$

$$Z_{Lj} = \frac{L_{Ej}}{\Delta t_i} \quad (3.7)$$

For small changes in voltages, the equivalent elements C_{Ej} , R_{Ej} and L_{Ej} will be constant. Hence

$$Z_{Cj} \propto \Delta t_i \quad (3.8)$$

$$Z_{Rj} = \text{constant} \quad (3.9)$$

$$Z_{Lj} \propto \frac{1}{\Delta t_i} \quad (3.10)$$

From this we see that if we repeat the numerical cycle three times with three different values of time increments $k_1 \Delta t_i$, $k_2 \Delta t_i$ and $k_3 \Delta t_i$ we will be able to get three values for each Z_j . By using the variation of the impedance factors with Δt_i noted in equations 3.8 to 3.10, we are able to write three equations

$$k_m Z_{Cj} + Z_{Rj} + \frac{Z_{Lj}}{k_m} = Z_{jm} \quad m = 1, 2, 3 \quad (3.11)$$

where Z_{jm} is the impedance factor found by using time interval $k_m \Delta t_i$. When $k_2 = 1.0$, the solution of these equations yields

$$Z_L = \frac{k_1 k_3}{k_1 - k_3} \left[\frac{Z_2 - Z_1}{1 - k_1} - \frac{Z_3 - Z_2}{k_3 - 1} \right] \quad (3.12)$$

$$Z_C = \frac{Z_3 - Z_2}{k_1 - 1} + \frac{Z_L}{k_3} \quad (3.13)$$

$$Z_R = Z_2 - Z_L - Z_C \quad (3.14)$$

The condition $\Delta Q_{ki} \gg \Delta Q_{Rki}$ can be realized by injecting into the top node a pulse which is much higher than the normal signal. Since this will result in large changes in voltages, all nonlinear elements must be temporarily replaced by a linear equivalent whose parameter values are the same as the incremental parameters of the nonlinear element during the last normal cycle. Because of these much higher than normal responses, one of these impedance factor calculation cycles cannot be used as a normal cycle in which time is incremented.

The second method of determining the impedance factors also depends on the assumed topology. If the circuit conforms to this topology, the various impedance factors are nothing more than the equivalent impedances looking from the point in question toward the reference node. If we recall that a node impedance factor Z_k was already defined, we can use this formula to calculate three impedances for the three time increments $k_1\Delta t_i$, Δt_i and $k_3\Delta t_i$. We can then again use equations 3.12 to 3.14 to calculate an equivalent capacitance C_E , resistance R_E and inductance L_E for the node. Since these are in series, they can be added to the corresponding elements in the branch above this node. In this way all the impedance factors may be calculated in a more direct manner than that of the first method. Since this last method is also much easier to program and much more conservative of computation time, in what follows it will be assumed that this latter method is being used to calculate the impedance factors.

At this point we might also introduce the conditions required to change the time increment during the process. We must impose the condition that during the time increment change the voltages across the three impedance factor elements defined in equations 3.2 to 3.4 remain constant:

$$v_{CEj} = C_{Ej} Q_j = \text{constant}$$

$$v_{REj} = R_{Ej} \frac{\Delta Q_j}{\Delta t} = \text{constant}$$

$$v_{LEj} = L_{Ej} \frac{\Delta^2 Q_j}{(\Delta t)^2} = \text{constant}$$

Since C_{Ej} , R_{Ej} and L_{Ej} are also constant during the increment size change, we conclude that the terms

$$Q_j, \quad \frac{\Delta Q_j}{\Delta t} \quad \text{and} \quad \frac{\Delta^2 Q_j}{(\Delta t)^2}$$

must also remain constant. This gives us our desired information.

4. VOLTAGE-CONTROLLED SUBNODES

In the previous formulation the current-controlled nonlinear element has a decided advantage since all the currents are determined before the branch and node voltages are calculated. In order to allow voltage-controlled devices to be handled just as efficiently it is desirable to formulate a similar process which will be compatible with the above but in which the role of the current and the voltage are interchanged. In this case we will allow KCL to be violated.

In the development of the relevant formulas we will assume that we are working with only one branch extracted from the circuit. To be as general as possible, we can postulate that this branch is made up of a series string of RLC elements as shown in Fig. 4.1. The current generator beside each parallel unit represents the error current for that unit. Since the nodes between the parallel units are associated only with branch j and do not have "levels" assigned to them, we will call them "voltage-controlled subnodes" to distinguish them from the normal nodes. To derive the necessary relations we must turn to the dual concept in which the flux is defined by

$$\varphi = \int_0^t v(t) dt \quad (4.1)$$

Then for linear elements we have

$$\varphi = LI$$

$$\frac{d\varphi}{dt} = RI \quad (4.2)$$

$$\frac{d^2\varphi}{dt^2} = \frac{1}{C} I$$

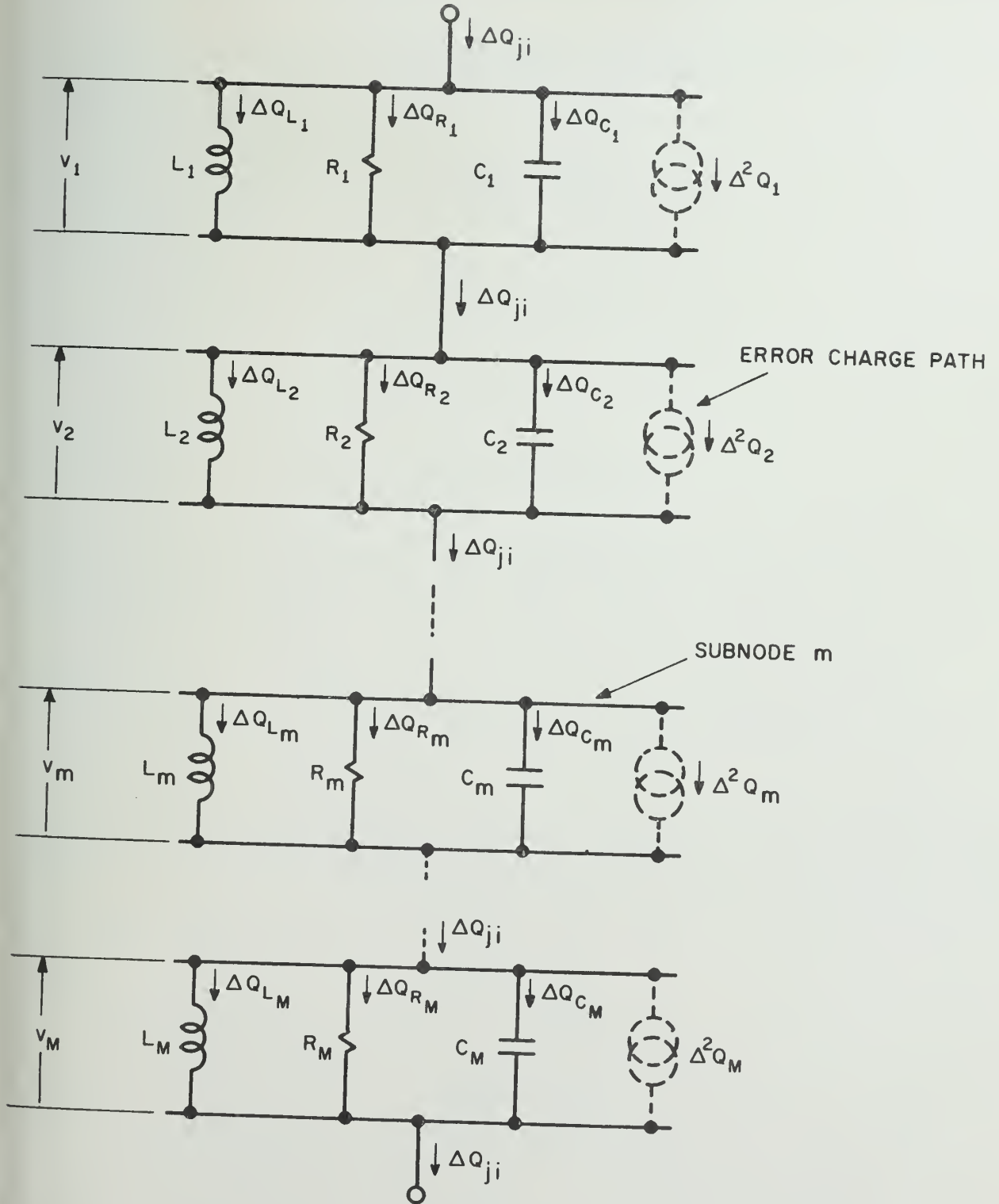


Figure 4.1. A Branch Consisting of M Voltage-Controlled Subnodes.

If we go to the difference notation we get for the mth parallel unit

$$\varphi_{mi} = \Delta Q_{mi} \frac{L_m}{\Delta t_i}$$

$$\Delta \varphi_{mi} = \Delta Q_{mi} R_m \quad (4.3)$$

$$\Delta^2 \varphi_{mi} = \Delta Q_{mi} \frac{\Delta t_i}{C_m}$$

where

$$\Delta \varphi_{mi} = \varphi_{mi} - \varphi_{m(i-1)}$$

$$\Delta^2 \varphi_{mi} = \Delta \varphi_{mi} - \Delta \varphi_{m(i-1)} \quad (4.4)$$

and

$$\Delta^3 \varphi_{mi} = \Delta^2 \varphi_{mi} - \Delta^2 \varphi_{m(i-1)}$$

These equations suggest that we define a set of "admittance factors" in a similar manner as the impedance factors were defined:

$$Y_{PL_m} = \frac{\Delta Q_{Lmi}}{\varphi_{mi}} \quad (4.5)$$

$$Y_{PR_m} = \frac{\Delta Q_{Rmi}}{\Delta \varphi_{mi}} \quad (4.6)$$

$$Y_{PC_m} = \frac{\Delta Q_{Cmi}}{\Delta^2 \varphi_{mi}} \quad (4.7)$$

$$Y_{Pm} = Y_{PLm} + Y_{PRm} + Y_{PCm} \quad (4.8)$$

where ΔQ_L , ΔQ_R , ΔQ_C are the charges flowing through the parallel L, R and C elements respectively. Also define

$$\Delta^2 Q_{mi} = \Delta Q_{ji} - \Delta Q_{mi} \quad (4.9)$$

where

$$\Delta Q_{mi} = \Delta Q_{Lmi} + \Delta Q_{Rmi} + \Delta Q_{Cmi}$$

$\Delta^2 Q_{mi}$ corresponds to Δv_{ji} in the main method.

Let us suppose that during the time interval (i-1) an error of

$\Delta^2 Q_{m(i-1)}$ resulted at subnode m. The condition for the compensation of this error in this step requires

$$(\Delta Q_{Lmi} - \Delta Q_{Lm(i-1)}) + (\Delta Q_{Rmi} - \Delta Q_{Rm(i-1)}) + (\Delta Q_{Cmi} - \Delta Q_{Cm(i-1)}) = \Delta^2 Q_{m(i-1)} \quad (4.10)$$

The amount of flux $\Delta^3 \phi_{Rmi}$ required to do this is given by

$$\Delta^3 \phi_{Rmi} = \frac{1}{Y_{Pm}} \left[\Delta^2 Q_{m(i-1)} - Y_{PLm} (\Delta \phi_{m(i-1)}) - (Y_{PLm} + Y_{PRm}) \Delta^2 \phi_{m(i-1)} \right] \quad (4.11)$$

This correction formula is analogous to that of equation 2.16 and hence can be treated with the same type of numerical procedure. Furthermore, any future comments on equation 2.16 can therefore also be applied with minor changes to equation 4.11. Further derivations parallel to those of sections 2.2 and 2.3 could be continued here which would then make it possible to work directly with such strings of parallel elements as shown in Fig. 4.1. However, in our method we can be content with just being able to handle one set of parallel elements.

The subscript m will be retained to distinguish charge in the voltage-controlled subnode from the other charges.

Besides equation 4.11 we also need a method of interconnecting the voltage-controlled node with the rest of the nodes of the circuit. To obtain this let us suppose that branch j which contains the voltage-controlled subnode has a set of impedance factors Z_{Cj} , Z_{Rj} and Z_{Lj} defined for it and is regarded by the charge distribution method of section 2.2 as a normal branch. After the charge distribution cycle a charge ΔQ_{ji} has been assigned to flow through branch j. The increase in charge

$$\Delta^2 Q_{ji} = \Delta Q_{ji} - \Delta Q_{j(i-1)}$$

can therefore be treated exactly the same as the error charge $\Delta^2 Q_{m(i-1)}$ and hence the two can be summed to form a total effective error charge of

$$\Delta^2 Q_{E m(i-1)} = \Delta^2 Q_{m(i-1)} + \Delta^2 Q_{ji} \quad (4.12)$$

Hence the increase in φ_m is determined by

$$\Delta^3 \varphi_{mi} = \frac{1}{Y_{Pm}} \left[\Delta^2 Q_{E m(i-1)} - Y_{PL}(\Delta \varphi_{m(i-1)}) - (Y_{PL} + Y_{PR})\Delta^2 \varphi_{m(i-1)} \right] \quad (4.13)$$

Since

$$v_{mi} = \frac{\Delta \varphi_{mi}}{\Delta t_i}$$

we get the prediction formula

$$v_{mi} = v_{m(i-1)} + \Delta v_{m(i-1)} + \frac{\Delta^2 Q_{E m(i-1)}}{Y_{Pm} \Delta t_i} - \frac{Y_{PLm}}{Y_{Pm}} v_{m(i-1)} - \frac{Y_{PLm} + Y_{PRm}}{Y_{Pm}} \Delta v_{m(i-1)} \quad (4.14)$$

where

$$\Delta v_{mi} = v_{mi} - v_{m(i-1)} \quad (4.15)$$

With this formula the voltage across the parallel elements can be calculated and consequently the currents through them can be obtained. The total charge ΔQ_{mi} can therefore be computed and the error charge for this cycle becomes

$$\Delta^2 Q_{mi} = \Delta Q_{ji} - \Delta Q_{mi} \quad (4.16)$$

After these calculations have been performed for all voltage-controlled subnodes, all branch voltages are known and therefore the node voltage calculation part of the numerical cycle can be started.

From the above it should be apparent that branch j which contains the voltage-controlled subnode can also have the full complement of series elements in addition to this subnode. This results because we essentially have two error-correcting mechanisms associated with branch j and therefore it can have two sets of elements, one in series and another in parallel.

By the use of this voltage-controlled subnode technique, restriction two of section 2.1 (only one branch can be connected between two nodes except if one of the nodes is the reference) is eliminated since we now have a method for dealing with parallel branches without violating the first restriction. Of course this technique is also useful for voltage-controlled elements since the voltage across the elements is first predicted and the currents are calculated later.

In section 2.2 we derived equation 2.16 which will compensate for a residual error between the branch and node voltages from the previous step. This formula was developed so that a circuit of the assumed topology and with correctly defined impedance factors will respond so as to have a zero resulting error between v_{ki} and v_{ji}^+ . If the impedance factors are not completely correct due to the presence of nonlinearities, equation 2.16 will not make the proper correction.

5.1 Error Term for a Branch

To find the factors related to this correction formula, let us examine the error that will be produced when the impedance factors are not correctly defined. To be able to do this we make the following assumptions:

- (1) The branch considered has impedance factors such that v_k is relatively independent of v_i^+ .
- (2) Z' , the impedance factor actually used, and Z , the correct impedance factor, are related by

$$Z' = Z + \Delta Z$$

where ΔZ is the error in Z' . Similar definitions hold for

$$Z'_C, Z_C, \Delta Z_C, Z'_R, Z_R, \Delta Z_R, Z'_L, Z_L \text{ and } \Delta Z_L$$

- (3) Q_{i-1} , ΔQ_{i-1} and $\Delta^2 Q_{i-1}$ are known.
- (4) The error voltage after the last step in the numerical process was

$$\Delta v_{(i-1)} = v_{k(i-1)} - v_{(i-1)}^+$$

(5) The node voltage v_k will be increased by an amount

$$\Delta v_{ki}.$$

The IQ method will then produce the terms

$$\Delta_{Ri}^{3Q'} = \frac{\Delta t}{Z'} \left(\Delta v_{(i-1)} - Z'_C \frac{\Delta Q_{(i-1)}}{\Delta t} - (Z'_R + Z'_C) \frac{\Delta^2 Q_{i-1}}{\Delta t} \right) \quad (5.1)$$

$$\Delta_{Ai}^{3Q'} = \frac{\Delta v_{ki} \Delta t}{Z'} \quad (5.2)$$

and

$$\Delta_{Qi}^{3Q'} = \Delta_{Ri}^{3Q'} + \Delta_{Ai}^{3Q'} \quad (5.3)$$

The correct third difference of charge should be

$$\Delta_{Ri}^{3Q} = \frac{\Delta t}{Z} \left(\Delta v_{i-1} - Z_C \frac{\Delta Q_{(i-1)}}{\Delta t} - (Z_C + Z_R) \frac{\Delta^2 Q_{i-1}}{\Delta t} \right) \quad (5.4)$$

$$\Delta_{Ai}^{3Q} = \frac{\Delta v_{ki} \Delta t}{Z} \quad (5.5)$$

The error is

$$\Delta_{Ei}^{3Q} = \Delta_{Qi}^{3Q} - \Delta_{Qi}^{3Q'} \quad (5.6)$$

By the substitution of appropriate definitions this becomes

$$\Delta_{Ei}^{3Q} = \frac{\Delta Z}{Z(Z + \Delta Z)} (\Delta v_{i-1} + \Delta v_{ki}) \Delta t + \frac{Z \Delta Z_C - Z_C \Delta Z}{Z(Z + \Delta Z)} \Delta Q_{i-1} + \frac{Z_L \Delta Z - Z \Delta Z_L}{Z(Z + \Delta Z)} \Delta^2 Q_{i-1} \quad (5.7)$$

The new error voltage for step (1) is given by

$$\Delta v_i = v_{ki} - v_i^+$$

By using previously derived relations we get

$$\Delta v_i = Z \frac{\Delta^3 Q_i}{\Delta t} \quad (5.8)$$

Hence

$$\Delta v_i = \frac{\Delta Z}{Z + \Delta Z} (\Delta v_{i-1} + \Delta v_{ki}) + \frac{Z \Delta Z_C - Z_C \Delta Z}{Z + \Delta Z} \frac{\Delta Q_{i-1}}{\Delta t} + \frac{Z_L \Delta Z - Z \Delta Z_L}{Z + \Delta Z} \frac{\Delta^2 Q_{i-1}}{\Delta t} \quad (5.9)$$

The first term indicates that if ΔZ is small, the error due to $(\Delta v_{i-1} + \Delta v_{ki})$ will be negligible. The second and third terms are directly related to the current and the current increase respectively in the branch. It may be observed that these can have much larger magnitudes than the first term. Nevertheless they do exhibit the convenient property of being slowly varying functions of time. This is a consequence of assuming that the impedance factors are relatively constant even though a nonlinear element may be present and that the current will normally not vary greatly from one numerical step to the next.

5.2 Compensation of the Error

The error caused by the last two terms in equation 5.9 is mostly attributable to the fact that the impedance factors were developed so that the circuit responds accurately to a pulse of width Δt which for linear elements connected in the assumed topology may be of any height. If a step function is applied, the circuit will respond accurately initially, but as the effects of the transient decrease, new impedance factors corresponding to longer Δt 's should

be used and eventually when the circuit is again in a steady state the impedance factors should merely be defined from the resistances of the circuit.

We note that as the effects of the transient are dying out the currents will become more and more constant from one step to another. Therefore the terms

$$\frac{Z\Delta Z_C - Z_C\Delta Z}{Z + \Delta Z} \frac{\Delta Q_{i-1}}{\Delta t} + \frac{Z_L\Delta Z - Z\Delta Z_L}{Z + \Delta Z} \frac{\Delta^2 Q_{i-1}}{\Delta t}$$

may be compensated by the introduction of a slowly time-varying factor into the correction formula. Since the error impedance factors of the form ΔZ are not known by the numerical process, this factor would have to be adjusted by observing the trend of the error voltage Δv_i and making changes to minimize Δv in the next few steps. The introduction of this adaptive variable eliminates the need of a multiplicity of impedance factors which would be impractical to use.

In the correction formula 2.16 we replace the term $\Delta v_{(i-1)}$ by $\Delta v_{(i-1)} + v_\alpha$ where v_α is the new factor mentioned above. Whenever the circuit is in a steady state, then at each branch

$$\Delta^2 Q_i \approx 0$$

$$\Delta v_i \approx 0$$

This requires that

$$v_\alpha = Z_C \frac{\Delta Q_i}{\Delta t} \quad (5.10)$$

When the transient analysis is started this condition must be forced and during transients v_α should be adapted so that when a steady state is reached this

condition will again hold. By the introduction of this correction factor the response of the circuit to the transients is in no way impaired; the impedance factors defined for Δt look after the fast transients and v_α adjusts the circuit to the slower transients.

It should be emphasized at this point that the error voltage Δv_i at each branch is known after each numerical step and hence can be controlled. If an error at a branch is too large, one can always repeat the step using a smaller time increment. Since Z_C varies directly with Δt and since the current $\frac{\Delta Q_i}{\Delta t}$ remains constant during the step size change the error term

$$Z_C \frac{\Delta Q_j}{\Delta t}$$

will also decrease with a decrease in the time interval. Hence the introduction of v_α is not absolutely necessary, but its use will increase the speed of computation considerably.

5.3 A Predictor-Corrector Type Method

To improve further the properties of the IQ method we can introduce a predictor-corrector type procedure which is somewhat analogous to those used in the integration of differential equations.^[6] We redefine the correction equation 2.16 as

$$\Delta_{Ri}^{3Qm} = \frac{\Delta t}{Z} \left[\Delta v_{Ei}^m - Z_C \frac{\Delta Q_{i-1}}{\Delta t} - (Z_C + Z_R) \frac{\Delta^2 Q_{i-1}}{\Delta t} \right] \quad m = 1, 2, \dots, M \quad (5.11)$$

where M is the number of times the process described in section 2 is repeated for each increment in time. The procedure is to calculate a value for Δv_{Ei}^1 for each node, use this in the distribution of the currents and calculate all

the node voltages. An error voltage Δv_i^1 will result which is then used to define a second value Δv_{Ei}^2 . This cycle is then repeated M times, the last being the one which will be accepted as yielding the charges and voltages for this time increment.

The problem is to determine a set of expressions for the terms Δv_{Ei}^m . This, in the general case, could become quite complicated but the results could prove to be valuable here in the same way as those obtained by including more terms in the predictor formulas in the integration of differential equations. To simplify matters we will restrict the discussion to the case in which $M = 2$, a value which would probably be close to the optimum when computation time versus decrease in error is considered. The expression for Δv_{Ei}^1 then has the form

$$\Delta v_{Ei}^1 = v_{\alpha} + a_1 \Delta v_{i-1}$$

a_1 can be either a constant for the branch or an adaptable factor which can be slowly adjusted during the analysis so that

$$\Delta v_i^1 \approx 0$$

The expression for Δv_{Ei}^2 becomes

$$\Delta v_{Ei}^2 = v_{\alpha} + a_1 \Delta v_{i-1} + a_2 \Delta v_i^1$$

where a_2 is again a constant or adaptable factor.

Since the three variable v_{α} , a_1 and a_2 all are directed towards decreasing the error Δv_i , it is obvious that they are highly interrelated. But, the role that they play is different: v_{α} is related to the algebraic sum of the error over a number of time intervals and a_1 and a_2 are related to the

numerical oscillations and damping. Since these parameters must be varied slowly, it is apparent that the numerical process must be slow enough to allow the adaptation of these parameters to the response.

This predictor-corrector type procedure was not studied further, but an analysis of the factors introduced and their relation to stability would probably prove useful.

6.1 Circuit Error and Response Error

Up to the present we have been talking about an error voltage Δv_i at each branch or an error current $\Delta^2 Q_i / \Delta t$ at a voltage-controlled subnode. For purposes of discussion we will call these the "circuit" errors. There is yet another type of error which we will name the "response" error. The latter refers to the difference between the theoretical value of a current or a voltage at a given time and the value of the same current or voltage obtained by the numerical process at the same time instance.

Previously it was shown that the circuit error can be controlled by specifying a maximum allowable error between any branch and the node to which it is connected. If we have K nodes connected in the worst case obtainable, namely all in series, and if at each node there is an error Δv_{\max} and since the voltage at the branch connected to the highest level node must be within $\pm \Delta v_{\max}$, we can conclude that the circuit error of any node voltage is less than $\frac{K}{2} \Delta v_{\max}$. Normally this error would be much smaller and in the specific case the exact upper bound can be determined from the topology of the circuit. We can also conclude that whenever the circuit is in a steady state the response error will be less than this maximum circuit error.

During transients the last statement does not hold, but we can define a rough estimate of the upper bound for the response error during the transient by considering the special case in which a linear capacitance is one of the branches below the node whose response error we wish to find. Suppose that the theoretical current flowing through the capacitance is given by $I(t)$ and that the current calculated by the IQ method is $\frac{\Delta Q_i}{\Delta t}$ where

$$i\Delta t < t < (i + 1)\Delta t$$

Also define

$$\frac{\Delta_E^2 Q_i}{\Delta t_i} = I(t) - \frac{\Delta Q_i}{\Delta t} \quad (6.1)$$

Then the error in the charge on the capacitance is

$$\Delta_E Q_i = \int_0^t I(t) dt - \sum_{m=1}^i \Delta Q_m = \sum_{m=1}^i \Delta_E^2 Q_m \quad (6.2)$$

If we assume $\Delta v_i = 0$ (i.e., $v_{ki} = v_i^+$), the response error becomes

$$\Delta v_{Ei} = \frac{1}{C} \Delta_E Q_i = \frac{1}{C} \sum_{m=1}^i \Delta_E^2 Q_m$$

But the maximum circuit error possible is Δv_{\max} and consequently

$$\frac{\Delta_E^2 Q_i}{C} < \Delta v_{\max}$$

If there is no cancellation of the circuit error from one time interval to another, we get the maximum response error

$$\Delta v_{Eimax} = i \Delta v_{\max}$$

In practical situations this would be much lower and furthermore a much closer upper bound for a specific circuit can be calculated by observing the circuit error at each time interval during the transient. From this it is also apparent that the adaptive factors v_α and a_1 should be adjusted so that small numerical oscillations will result. This will cause the circuit error to oscillate between positive and negative values and therefore produce a much smaller response error. It is also felt that a much lower upper bound for the response error could be arrived at if the energy conservation criterion is used to calculate the node voltage, but this was not examined.

6.2 Stability

The stability of the IQ method has not yet been examined in detail, but from the discussion of errors we can make a few observations about stability. First let us recall that in the normal predictor-corrector methods of numerical analysis there is available an error term which is used to control the increment. Consider the example

$$\text{Predictor} \quad x_{pi} = x_{c(i-1)} + \Delta t \dot{x}_{c(i-1)}$$

$$\text{Corrector} \quad x_{ci} = x_{c(i-1)} + \frac{\Delta t}{2} (\dot{x}_{pi} + \dot{x}_{p(i-1)})$$

where the term $(x_{ci} - x_{pi})$ is the error. It is to be noted that this is a relative error since the corrected as well as the predicted value may be erroneous. When both terms are in error but the difference between them is small, the solution will possibly become numerically unstable.

On the other hand, in the IQ method the error which controls the step size is the circuit error, an absolute error. We have already seen that we can set an upper bound for this error. Since we can assume the circuit error is initially within the allowed bounds, then for each succeeding step the error will also be within these bounds. The last statement is justified if we assume that there are no discontinuities in any v-i characteristics and if we recall that a decrease in the time increment implies a decrease in the circuit error. Therefore as long as we have continuous functions for the v-i characteristics the solution will not be able to "blow up."

The problem of instabilities in the integration of the differential equations of a circuit are usually related to the minimum time constants of the circuits which will cause instabilities if the time increment is too

large.^[1] For the IQ method this does not appear to be a problem. Consider for example the branch in Fig. 6.1 which has a very low series inductance and a high resistance:

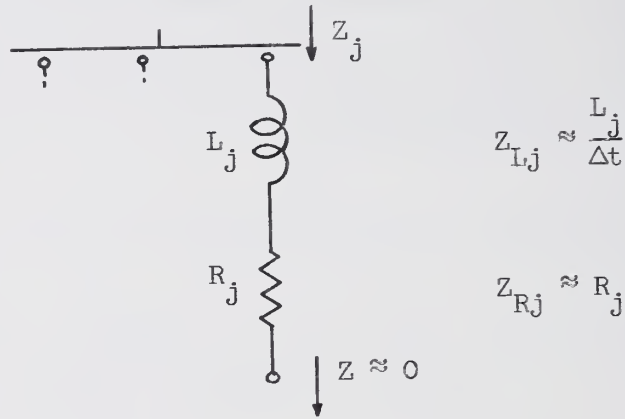


Figure 6.1.

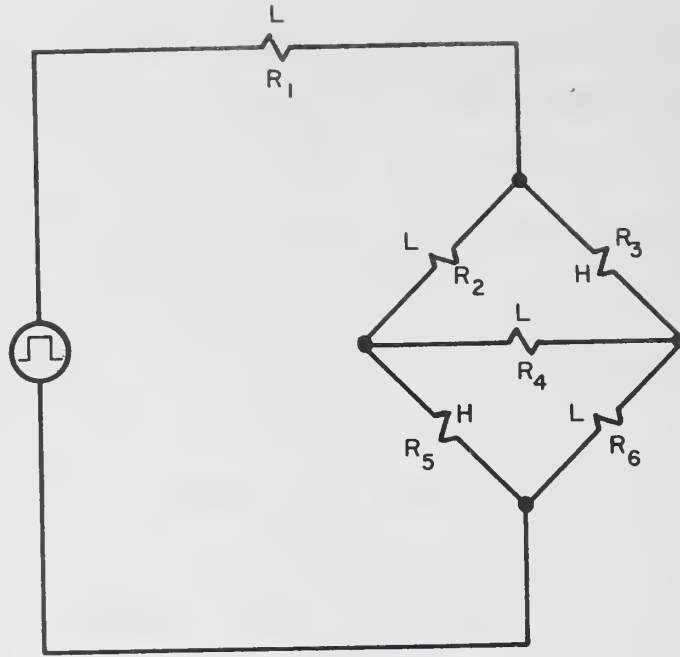
If the node voltage varies slowly with time and a large Δt is being used then Z_L is insignificant compared to Z_R and consequently Z_L is all but ignored by the method. If a large transient (with a finite slope) appears at the node, Δt will be decreased until the node voltage change is only incremental. Now Z_L has a much higher value and might even dominate Z_R . As the transient disappears, Δt is again increased in size and Z_L again assumes an insignificant role. Thus we see that the small inductance will only have an effect on the circuit during fast transients.

7. RELAXATION OF TOPOLOGICAL RESTRICTIONS

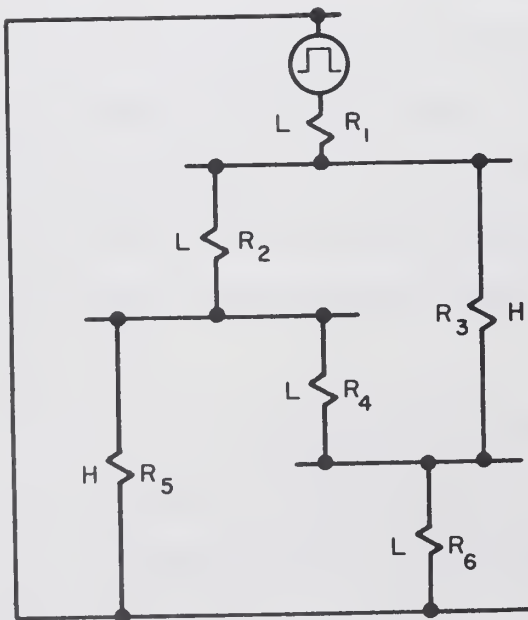
Suppose that it is desired to perform an analysis of a bridge type circuit shown in Fig. 7.1a. The elements marked L are assumed to be lower impedances (e.g., 10 ohms) than those marked H (1000 ohms). Two possible redrawings of the circuit according to the method described appear in Figs. 7.1b and 7.1c. Both forms of the circuit can be analyzed by the IQ method but for fast transients considerably more difficulty will be experience with Fig. 7.1c than with Fig. 7.1b. It may be recalled that the impedance factors were derived from the "down-directed" equivalent impedances. The impedance factor at the top node would therefore be approximately 40 ohms for Fig. 7.1b and about 500 ohms for Fig. 7.1c, whereas the correct impedance is a little less than 40 ohms. If a voltage step is applied to the circuit of Fig. 7.1c, the injected current will be grossly underestimated and the process of establishing equilibrium would take much longer than in the case of Fig. 7.1b where it would be established in very few numerical cycles.

The conclusion from the above is that if a circuit does not have the desired topology a wise rearrangement of the circuit will possibly make it amenable to as fast a solution as that of a circuit which has the restricted topology. There seem to be a few general rules which will usually lead to convenient configurations if the original circuit does not have the desired topology:

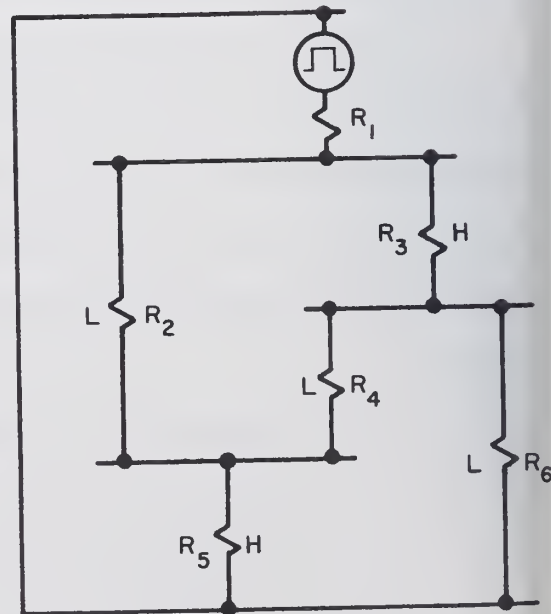
- (1) If possible the highest level node influencing the portion of the circuit with the undesirable topology should have as low an impedance path to the reference as obtainable.
- (2) If possible the circuit should be arranged so that the lowest impedance branches lead to the lowest possible node levels.



a) ORIGINAL



b) CORRECT REDRAWING



c) WRONG REDRAWING

Figure 7.1. Example of a Circuit Violating the Assumed Topology.

By allowing these variations in the topology, we must also restrict the forcing function voltage to incremental changes from one time interval to the next since the impedance factors will no longer give the exact response to a high pulse. In a specific circuit the amount of difficulty the method will encounter can be predicted since it is directly related to how well the impedance factors approximate the actual equivalent impedances.

8.1 Sources

A voltage source is already included in the IQ method and a constant current source does not present any difficulties since this requires only that a charge $I_0 \Delta t$ be subtracted from one node and added to another before the start of the charge distribution cycle. With constant sources there are no problems (except possibly during the initialization) but if they are time-dependent or proportional to currents or voltages in another part of the circuit the method might have trouble. If a voltage source, for instance, is time-dependent and during one numerical cycle experiences a large change, this change will not be taken into account by the first charge distribution cycle since no impedance factors are changed. When the node voltages are then calculated there will be a large error at the branch with the voltage source. Since this error will then be diminished by the next numerical cycle through the error-correction mechanism, we see that the response of the circuit to all varying voltages will be delayed one cycle. A current source will also produce the same result, but with the slight advantage that the node to which it is connected will respond immediately and the delay will appear in a higher level node. This advantage can often be put to good use. The rule in general seems to be that only incremental changes should be allowed from one time interval to another for varying sources.

8.2 Nonlinear Elements

In general we can specify the characteristics of a nonlinear element by

$$\frac{\Delta^m Q}{(\Delta t)^m} = f(v) \quad \text{or} \quad v = g \left(\frac{\Delta^m Q}{(\Delta t)^m} \right) \quad m = 0, 1 \text{ or } 2 \quad (8.1)$$

The second form is the one which falls naturally into the domain of the IQ method but unfortunately it is not always the most convenient to use. For instance, in a tunnel diode the relation

$$v = g\left(\frac{\Delta Q}{\Delta t}\right)$$

is multivalued. In such cases the voltage-controlled node formulas developed earlier can be used in conjunction with the first of the above formulas which is in this case single valued. The important thing is that the prediction and circuit-error correction mechanism is supplied by the method, therefore avoiding the need of a repetitious process such as Newton's method to determine the independent variable when the dependent variable is given. This can prove to be an important time-saving factor during computation.

8.3 Semiconductor Diodes

Since the diode and transistor are the most important nonlinear elements, they will be discussed here in more detail. The dc characteristics of an ideal diode are given by

$$I = I_0 \left[e^{\frac{v}{\lambda}} - 1 \right] \quad \lambda = \frac{kT}{q} \quad (8.2)$$

The incremental conductance is given by

$$g_D = \frac{dI}{dv} = \frac{I_0}{\lambda} e^{\frac{v}{\lambda}} \quad (8.3)$$

During the transients the incremental diode capacitance given by

$$C = \frac{dQ}{dv} \quad (8.4)$$

also becomes important. When in the nonconducting region the diode exhibits a depletion layer capacitance of the form

$$C_c = \frac{C_0}{(1 + \frac{v}{v_D})^n} \quad (8.5)$$

where v_D is the built-in potential, n is the grading constant which is usually equal to $\frac{1}{2}$ or $\frac{1}{3}$ and C_0 is a constant.

The diffusion type capacitance when in the conduction region is

$$C_D = \frac{dQ}{dv} = g_D \frac{dQ}{dI} \quad (8.6)$$

The term $\frac{dQ}{dI}$ is a time constant which can usually be assumed constant as a first approximation and equal to the diode constant τ_D . Hence

$$C_D \approx g_D \tau_D \quad (8.7)$$

Normally only one of the two capacitances will be important in a particular application. In switching circuits C_D is most important and usually C_c is small enough that it can be approximated by a constant.

If τ_D cannot be considered a constant the relation $Q = f(v)$ must be obtained by numerical integration during the transient:

$$Q = \int_0^v C_D(v) dv = \int_0^v g_D(v) \tau_D(v) dv \quad (8.8)$$

If τ_D can be assumed constant we get the relation

$$Q = \tau_D I_0 e^{\frac{v}{\lambda}} \quad (8.9)$$

When the depletion layer capacitance parameters v_D , n and C_0 can be assumed constant, and if the diode is reverse biased, we get the formula

$$Q = \frac{\lambda}{n - n^2} \left[\left(1 - \frac{v}{v_D}\right)^n - \left(1 - \frac{v}{v_D}\right) \right] C \quad (8.10)$$

From a programming point of view the expressions for I , g_D , C and Q are in a very convenient form since they are so highly interrelated. This gives the very important result that no further simplifying assumptions which are usually made in a normal analysis will be required.

To complete the model for the diode we can include the leakage resistance R_C and if the reverse breakdown is important, a current of the form

$$I_B = \frac{I_0}{1 - \left(\frac{v}{v_B}\right)^n} \quad (8.11)$$

where

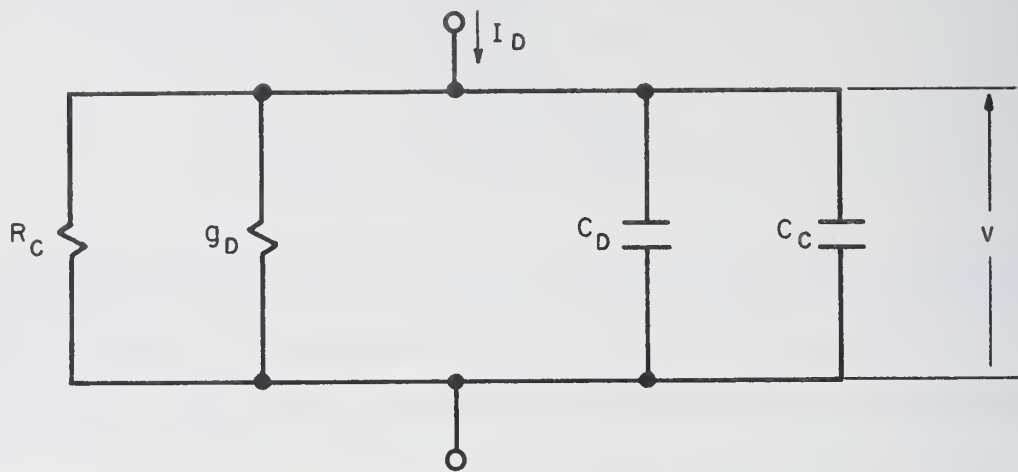
$$\frac{1}{1 - \left(\frac{v}{v_B}\right)^n}$$

is the multiplication factor and v_B is the reverse breakdown voltage.

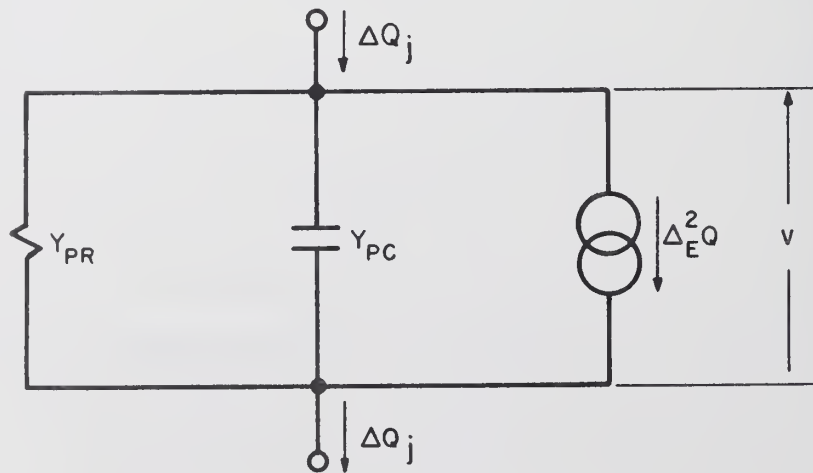
Since all the above elements are in parallel and since the current equation is in the form

$$\frac{\Delta Q}{\Delta t} = f(v)$$

we must use the voltage-controlled subnode method. The relevant parameters are given by



a) IN TERMS OF DIODE PARAMETERS



b) IN TERMS OF ADMITTANCE FACTORS

Figure 8.1. Semiconductor Diode Model.

$$Y_{PL} = 0 \quad Y_{PR} = g_D + \frac{1}{R_c} \quad (8.12)$$

$$Y_{PC} = \frac{C}{\Delta t} \quad Y_P = g_D + \frac{1}{R_c} + \frac{C}{\Delta t}$$

The prediction formula 4.14 therefore reduces to

$$v_i = v_{i-1} + \Delta v_{(i-1)} + \frac{\Delta^2 Q_{(i-1)}}{Y_P \Delta t} - \frac{Y_{PR}}{Y_P} \Delta v_{(i-1)} \quad (8.13)$$

The spreading resistance and the wiring inductance have not yet been included, but these present no problem since we can still specify a complete set of series elements for the branch containing the diode.

8.4 Transistors

Of the different large signal models available for the transistor, it was found that for the IQ method the Ebers and Moll model gives the best balance between accuracy and efficiency in computation. For this reason the technique available to handle this model will be developed in detail.

The equations of a PNP transistor for the dc case are

$$I_E = - \frac{I_{EO}}{1 - \alpha_N \alpha_I} \left(e^{\frac{qV_E}{kT}} - 1 \right) + \alpha_I \frac{I_{CO}}{1 - \alpha_N \alpha_I} \left(e^{\frac{qV_C}{kT}} - 1 \right) \quad (8.14)$$

$$I_C = \alpha_n \frac{I_{EO}}{1 - \alpha_N \alpha_I} \left(e^{\frac{qV_E}{kT}} - 1 \right) - \frac{I_{CO}}{1 - \alpha_N \alpha_I} \left(e^{\frac{qV_C}{kT}} - 1 \right) \quad (8.15)$$

The notation and the sign convention is that used by Ebers and Moll^[4] with the exception that the symbol ϕ is replaced by v . Therefore these will not be

discussed here in detail. For future convenience let us make the following definitions:

$$\lambda = \frac{kT}{q}$$

$$I_{EFO} = \frac{-I_{EO}}{1 - \alpha_N \alpha_I}$$

$$I_{EF} = I_{EFO} \left(e^{\frac{v_E}{\lambda}} - 1 \right)$$

$$I_{CFO} = \frac{-I_{CO}}{1 - \alpha_N \alpha_I}$$

$$I_{CF} = I_{CFO} \left(e^{\frac{v_C}{\lambda}} - 1 \right)$$

Therefore

$$I_E = I_{EF} - \alpha_I I_{CF} \tag{8.16}$$

$$I_C = -\alpha_N I_{EF} + I_{CF}$$

A conductance for the emitter junction and one for the collector junction are defined as follows:

$$g_E = \left(\frac{\delta I_E}{\delta v_E} \right) \bigg|_{v_C = \text{const}} = \frac{I_{EF} + I_{EFO}}{\lambda} \tag{8.17}$$

$$g_C = \left(\frac{\delta I_C}{\delta v_C} \right) \bigg|_{v_E = \text{const}} = \frac{I_{CF} + I_{CFO}}{\lambda}$$

When the junctions are reverse biased the leakage resistance R_E and R_C for the emitter and collector junctions respectively become important and therefore must be included in the equivalent circuit.

During transients either a diffusion capacitance or a depletion layer capacitance come into play at each junction, depending on whether the junction is forward or reverse biased. The two diffusion capacitances which are characterized by two time constants τ_E and τ_C are given by

$$\begin{aligned} C_{DE} &= \tau_E g_E \\ C_{CE} &= \tau_C g_C \end{aligned} \tag{8.18}$$

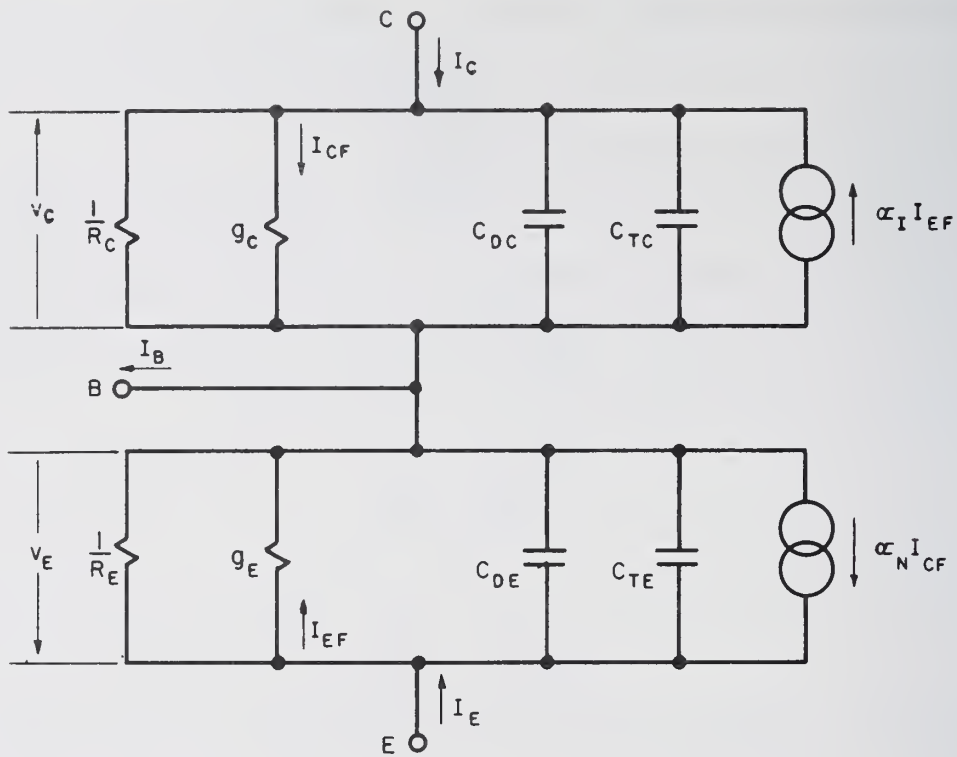
The time constant τ_E and τ_C can be assumed constant as a first approximation and therefore similar charge versus voltage relations as equation 8.9 for diodes can be obtained. The depletion layer capacitances are given by

$$\begin{aligned} C_{TE} &= \frac{C_{OE}}{\left(1 - \frac{v_E}{v_{DE}}\right)^{n_E}} \\ C_{TC} &= \frac{C_{OC}}{\left(1 - \frac{v_C}{v_{DC}}\right)^{n_C}} \end{aligned} \tag{8.19}$$

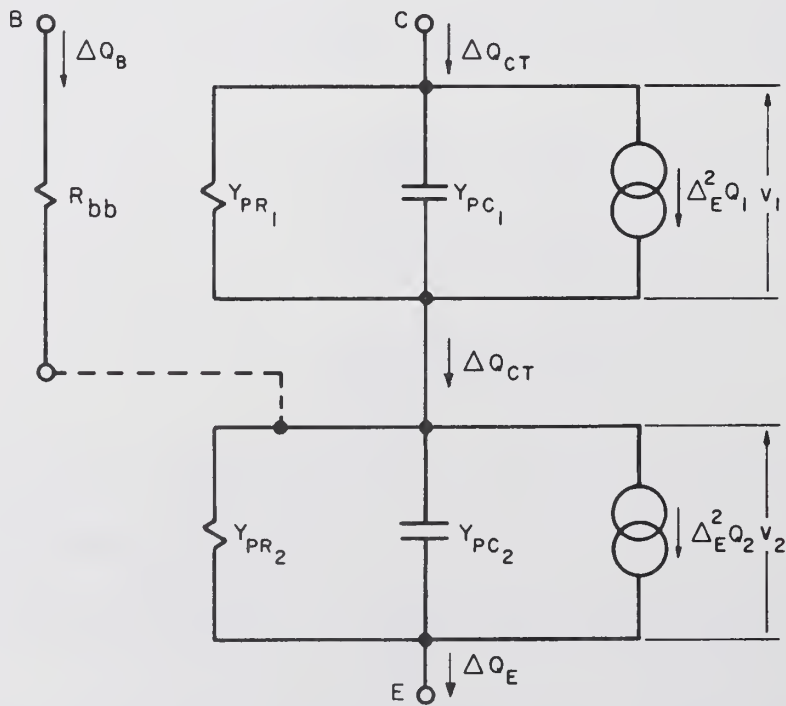
where C_{OC} and C_{OE} are constants of the transistor, v_{DE} and v_{DC} are the built-in potentials for the emitter and collector junctions and n_E and n_C are grading constants.

Combining all of the above we have the model shown in Fig. 8.2a.

The reason for the unusual orientation will become apparent later. We note two important properties of this equivalent circuit: the collector and the emitter junctions have the same configurations and similar elements as the



a) IN TERMS OF TRANSISTOR PARAMETERS



b) IN TERMS OF ADMITTANCE FACTORS

Figure 8.2. IQ Model of a Transistor.

equivalent circuit for the diode except for the current generator, and the circuit is in the exact form required by the voltage-controlled subnode method of section 4. The first of the above indicates that we could easily use the method developed for diodes in section 8.3. But, the second property suggests that a more general technique designed specifically for transistors can be formulated.

Since we have no inductive element in the circuit, equation 4.11 reduces to

$$\Delta^3 \varphi_{mi} = \frac{1}{Y_{Pm}} \left[\Delta^2 Q_{m(i-1)} \right] - \frac{Y_{PRm}}{Y_{Pm}} \Delta^2 \varphi_{m(i-1)} \quad (8.20)$$

To put this in terms of voltages we invoke the relations

$$v = \frac{\Delta \varphi}{\Delta t} \quad \Delta v = \frac{\Delta^2 \varphi}{\Delta t} \quad \Delta^2 v = \frac{\Delta^3 \varphi}{\Delta t} \quad (8.21)$$

Therefore

$$\Delta^2 v_{mi} = \frac{\Delta^2 Q_{m(i-1)}}{Y_{Pm} \Delta t} - \frac{Y_{PRm}}{Y_P} \Delta v_{m(i-1)} \quad (8.22)$$

For the transistor we have two parallel units, unit 1 at the collector junction and unit 2 at the emitter junction. The admittance factors for these two units are defined by

$$\begin{aligned} Y_{PR1} &= g_C + \frac{1}{R_c} \\ Y_{PC1} &= \frac{C_{TC}}{\Delta t} + \frac{C_{DC}}{\Delta t} \\ Y_{P1} &= Y_{PR1} + Y_{PC1} \end{aligned} \quad (8.23)$$

$$Y_{PR2} = g_E + \frac{1}{R_E}$$

$$Y_{PC2} = \frac{C_{DE}}{\Delta t} + \frac{C_{TE}}{\Delta t} \quad (8.24)$$

$$Y_{P2} = Y_{PR2} + Y_{PC2}$$

The voltages are given by

$$v_{1i} = v_{ci} = v_{1(i-1)} + \Delta v_{1(i-1)} + \Delta^2 v_{1i} \quad (8.25)$$

$$v_{2i} = -v_{Ei} = v_{2(i-1)} + \Delta v_{2(i-1)} + \Delta^2 v_{2i}$$

The two current generators $\alpha_I I_{EF}$ and $\alpha_N I_{CF}$ can be absorbed into the "error" current generators $\Delta^2 Q_1 / \Delta t$ and $\Delta^2 Q_2 / \Delta t$. It may be recalled that $\Delta^2 Q_m$ was the error charge as defined in equation 4.9 and ΔQ_m was the sum of the charges flowing through the parallel R, L and C elements. For the transistor the relations become

$$\Delta^2 Q_1 = \Delta Q_{CT} - \Delta Q_1$$

$$\Delta^2 Q_2 = \Delta Q_{CT} + \Delta Q_B - \Delta Q_2$$

where ΔQ_{CT} and ΔQ_B are defined in Fig. 8.2b and ΔQ_1 and ΔQ_2 are given by

$$\Delta Q_1 = \frac{v_1}{R_C} + I_{CF}(v_1) + C_{DC} \frac{\Delta v_1}{\Delta t} + C_{TC} \frac{\Delta v_1}{\Delta t} - \alpha_I I_{EF} \Delta t \quad (8.26)$$

$$\Delta Q_2 = \frac{v_2}{R_C} + I_{EF}(-v_2) + C_{DE} \frac{\Delta v_2}{\Delta t} + C_{TE} \frac{\Delta v_2}{\Delta t} + \alpha_N I_{CF} \Delta t \quad (8.27)$$

There is still one remaining inconvenience which concerns timing. If the normal IQ procedure is followed, the current will first be distributed and therefore at the transistor we get the terms

$$Q_{CTi} = Q_{CT(i-1)} + \Delta^2 Q_{CTi}$$

$$Q_{Bi} = Q_{B(i-1)} + \Delta^2 Q_{Bi}$$

The error term which is to be used in equation 8.22 then becomes

$$\Delta^2 Q_{1i} = \Delta^2 Q_{1(i-1)} + \Delta^2 Q_{CTi} \quad (8.28)$$

$$\Delta^2 Q_{2i} = \Delta^2 Q_{2(i-1)} + \Delta^2 Q_{Bi} + \Delta^2 Q_{CTi}$$

If the new voltages v_{1i} and v_{2i} are calculated from this, there is a possibility of a larger error in ΔQ_1 and ΔQ_2 since the correction formula does not take into account the fact that $\alpha_{I_{EF}} \Delta t$ and $\alpha_{N_{CF}} \Delta t$ will have different values in time interval i from those in time interval $(i-1)$. Consequently the two current generators will always be lagging behind the voltages by one numerical cycle during transients. To compensate for this, values for v_{1i} and v_{2i} can be predicted from errors in interval $(i-1)$ and these may then be used to predict values for $\alpha_{I_{EF}} \Delta t$ and $\alpha_{N_{CF}} \Delta t$ for the time interval i . The changes from interval $(i-1)$ to i can then be included in the error formulas 8.28. It is also apparent that a predictor-corrector type method such as described in section 5.3 could be used here to further reduce this numerical lag effect.

To see how the transistor equivalent is incorporated into the rest of the circuit we must recall the assumption that only one branch of the main circuit is involved when dealing with a set of voltage-controlled subnodes. Hence the entire equivalent for the transistor except the base is included in one

branch. The collector bulk resistance R_{cc} and any possible lead inductance can, as with the diode, be specified in the series elements associated with this branch. A second branch is required for the base and therefore it would contain the base resistance R_{bb} . Since the voltage-controlled subnodes such as that in the center of the transistor model are normally not available to the main IQ method, a special set of nodes, one per transistor, must be defined so that the channeling of the charge which flows through the base branch to the internal transistor subnode can be accomplished.

The orientation of the transistor equivalent shown in Fig. 8.2 is mainly for purposes of being able to determine the approximately correct impedance factors and to help prevent the current generator lags mentioned above. The parallel admittances of the transistor equivalent can be converted to series impedance factors by the method described in section 3. These are illustrated in Fig. 8.3. Normally Z_E would be fairly small and capacitive

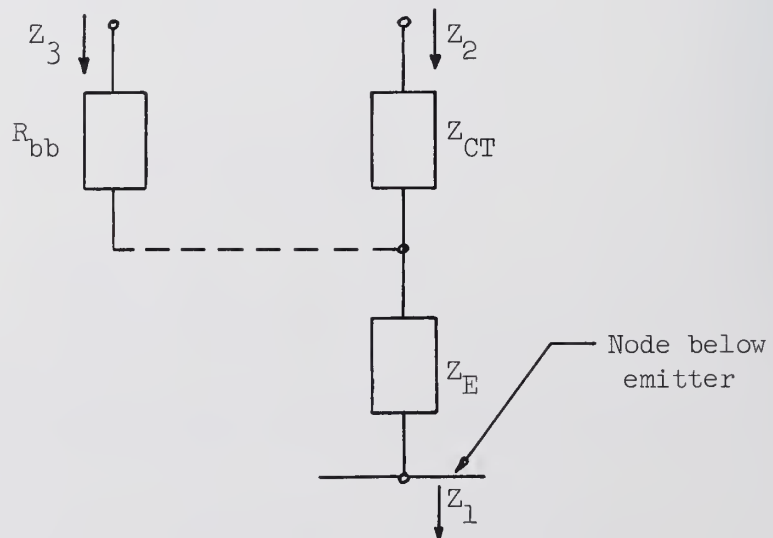


Figure 8.3

because of a large C_{DE} , and Z_{CT} would be large except when the transistor is in saturation. Thus if Z_1 is small the values determined by the impedance factor calculation method of section 3 will be

$$Z_2 = Z_1 + Z_E + Z_{CT} \approx Z_{CT} \quad (8.29)$$

$$Z_3 = Z_1 + Z_E + R_{bb} \quad (8.30)$$

Because of the normally high value of Z_{CT} as compared with R_{bb} , the defined impedance factors are a good approximation of the actual ΔQ versus Δv behavior at the transistor terminals. Therefore this orientation of the transistor equivalent will normally be used. As an example of how a transistor circuit would be redrawn before analysis by the IQ method, an asymmetric flipflop circuit is shown in Fig. 8.4.

8.5 Transmission Lines

When working with high-speed circuitry one invariably meets a situation in which a signal delay is involved. Since an equivalent transmission line will usually represent the phenomenon adequately, a technique by which the IQ method can handle transmission lines will be briefly discussed.

Consider the lossless transmission line of Fig. 8.5a. It was found that the most convenient equivalent circuit is that shown in Fig. 8.5b. Z_0 is the characteristic impedance of the line and the forward and reverse currents at the sending and receiving end are defined as follows:

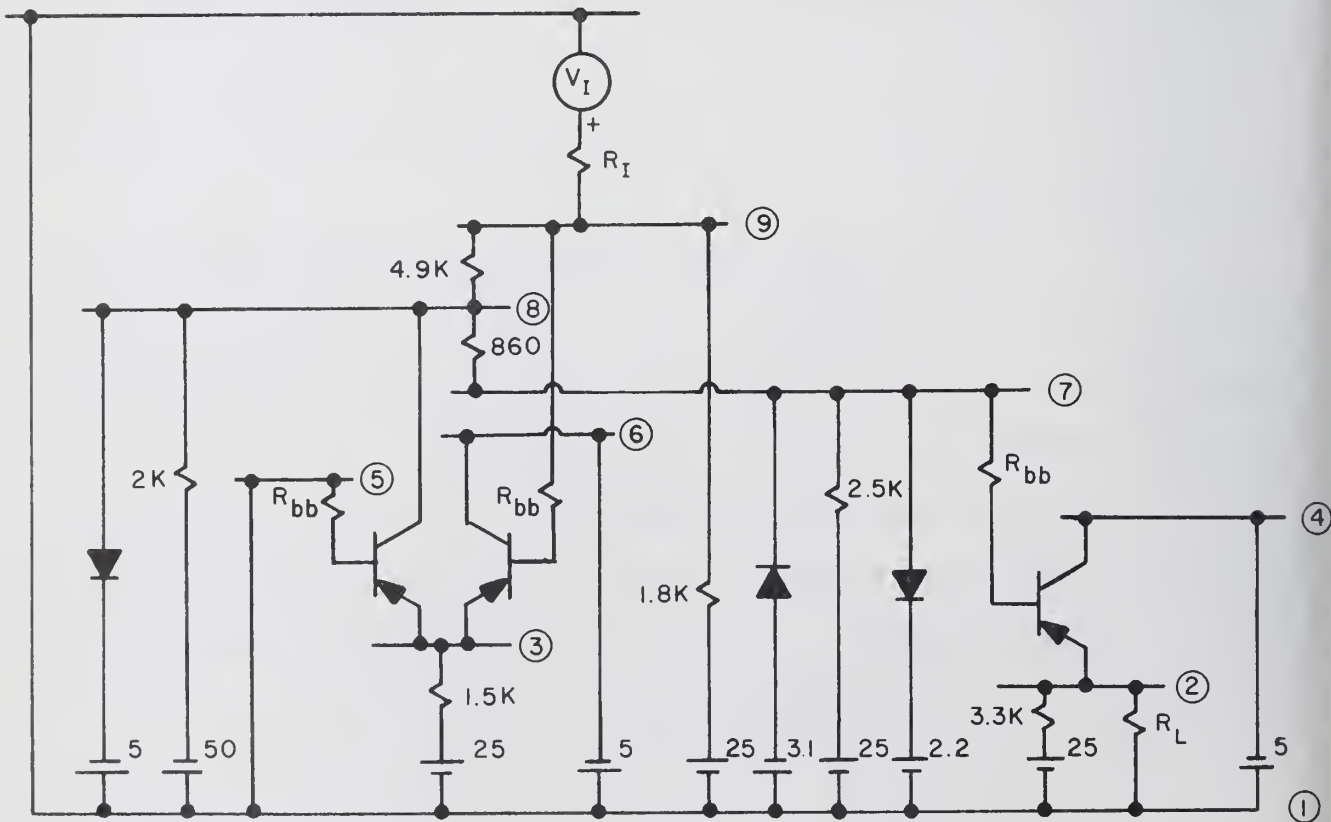
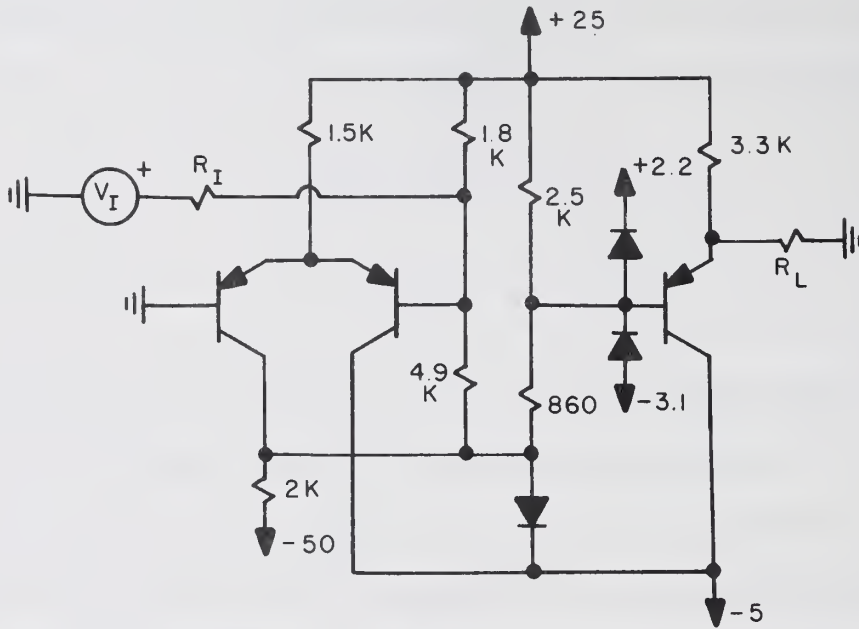
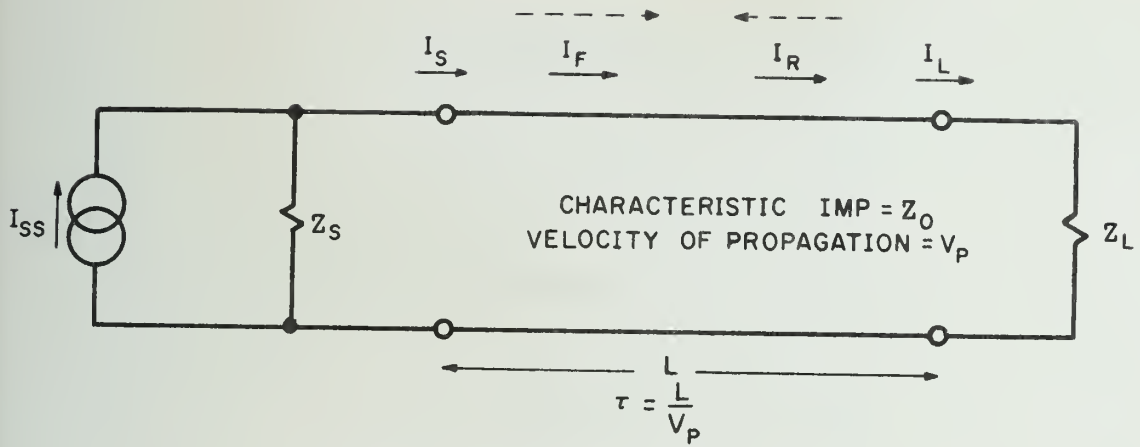
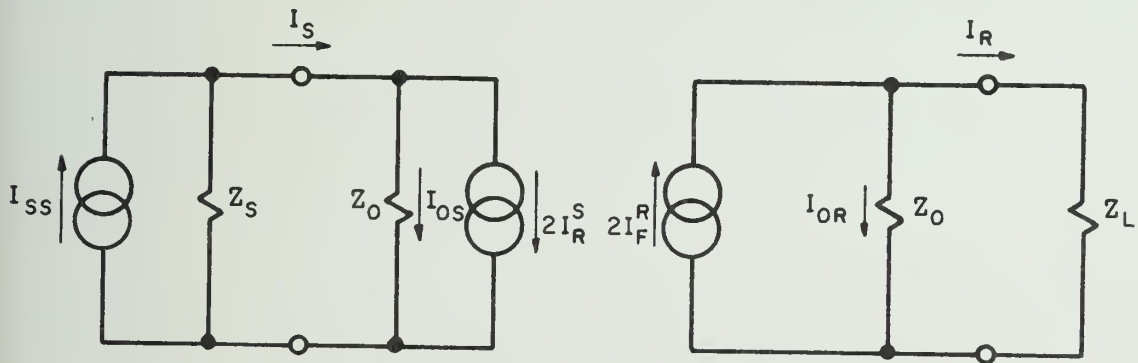


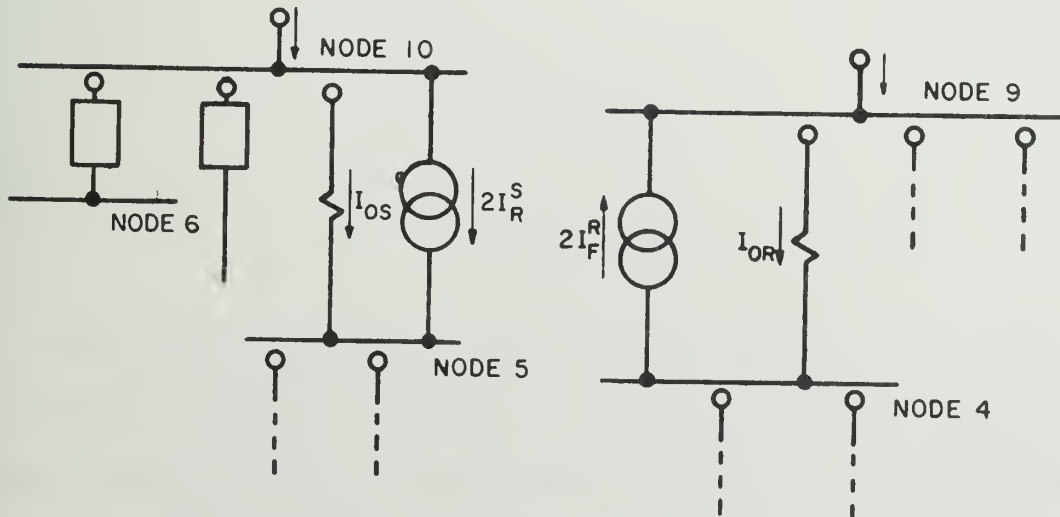
Figure 8.4. Asymmetric Flipflop Example.



a) ACTUAL TRANSMISSION LINE



b) EQUIVALENT CIRCUIT



c) A TRANSMISSION LINE IN A CIRCUIT

Figure 8.5. Transmission Line and Equivalent

$$I_F^S = I_F \quad \text{at the sending end}$$

$$I_F^R = I_F \quad \text{at the receiving end}$$

(8.31)

$$I_R^R = I_R \quad \text{at the receiving end}$$

$$I_R^S = I_R \quad \text{at the sending end}$$

We therefore have the following relations:

$$I_S = I_F^S + I_R^S \quad \text{and} \quad I_L = I_F^R + I_R^R \quad (8.32)$$

$$I_F^R(t) = I_F^S(t - \tau)$$

(8.33)

$$I_R^S(t) = I_R^R(t - \tau)$$

By imposing boundary conditions so that the reflection coefficients are correctly defined we get

$$I_F^S = I_R^S + I_{OS}$$

(8.34)

$$I_R^R = I_F^R - I_{OR}$$

From the previous set of definitions we see that I_R^S and I_F^R are the delayed forward and reverse currents respectively and therefore are known quantities at any time instance. If the equivalent impedances of the line at the sending and receiving ends are treated as normal branches by the IQ method, I_{OS} and I_{OR} will be known after the current distribution cycle. Consequently the currents I_F^S and I_R^R which are to be entered into the two delay tables are easily calculated. These emerge after a time τ as the values for I_F^R and I_R^S respectively.

The above can also be adapted to lossy transmission lines, the difference being that now the data in the delay tables must be processed in some manner instead of being merely stored. Since this is out of the domain of this report, the subject will not be discussed further.

Although the above relations for the transmission line are very simple, two complications enter during implementation. Since the delay tables must be of fixed size there is a problem of matching the fixed Δt of the line to the variable time increment which is possible in the IQ method. This problem is fairly easily solved by integrating the charge entering the line when the line Δt is larger than the IQ time increment and by "filling" the spaces in the table which are not used when the line Δt is smaller than the IQ time increment. The second problem is one of initializing the delay tables. Since points 1 and 3, and 2 and 4 in Fig. 8.5 are parts of the same node at dc, they should also be treated by the IQ method as the same nodes but this presents some problems which have not yet been completely resolved and which are directly related to how the main IQ method is programmed. However, this problem also does not seem to be insurmountable.

9.1 The Program

To verify some of the ideas contained in the above, a program based on the IQ method was written. Although the time element prevented the inclusion of all of the techniques developed, the basic ideas of sections 2 and 3 were all included. In addition a method for handling nonlinear two-terminal devices such as tunnel diodes and the method for analyzing transmission lines were incorporated into the program. Since some major changes in the organization of the program would be required to include efficiently the voltage-controlled subnode method, the addition of this and hence the model for the diode and transistor has not yet been completed. The program was written in FORTRAN II for the IBM 7094 system at the Digital Computer Laboratory, University of Illinois.

The input part of the program is written in such a manner that the sequence in which the nodes are read automatically defines their level. For each node the numbers of all the branches below the node are also read from the tape. The branch data read in by the program consists of the node number below the branch, the four constants of the branch and if it has a nonlinear element, the type and number of the nonlinearity. The rest of the data is read by the program in a standard manner.

The main part of the program consists of routines for inputting and outputting data, incrementing circuit variables and for the actual calculation of the response. A simplified flow chart of the latter is shown in Fig. A-1 of the appendix. After initializing of the table, the dc initial conditions are evaluated. Since this uses the same routines as the transient analysis with minor changes, the program is put in "Mode 1" during the dc calculations. While in this mode, the subroutines will replace all capacitances by open

circuits and all inductances by shorts, which leads to a relaxed condition when the dc analysis is completed. Other initial conditions could be easily specified by making minor changes in the program, but these have not yet been programmed. Initially all sources have zero values; then the program "turns them on" by successively increasing the values of the sources until they have their desired values, meanwhile continually solving the circuit to prevent large discontinuities. This process does not seem to take excessive time; yet it allows bistable circuits to be set as desired. This part of the program in itself provides a means for the dc analysis of nonlinear circuits.

When the dc initialization is completed, Mode 2 is set and the transient analysis is started. The control of the printing, time incrementing and impedance calculation is shown in the right half of Fig. A-1. QV is the name of the subroutine which distributes the charge and calculates the node voltages, IMP calculates the impedance factors and ALTERT changes the time increment and checks if the present set of values is to be printed. The simplified flow charts of IMP and ALTERT are found in Figs. A-4 and A-5. The terms found in Fig. A-5 are defined by the following:

DT --Present time increment
TMAX --Time at which analysis is stopped
DTM --Minimum time increment allowed
DVM --Maximum node voltage increase during cycle
DVU --Maximum node voltage increase allowed
DVL --If DVM is less than this the time increment can be doubled

It is to be emphasized again that the flow charts do not represent the subroutines exactly; their purpose is merely to present some of the major computational steps in the subroutines.

Figures A-2 and A-3 contain the charge distribution and node voltage calculation loops which will require the most computer time during the analysis. The flow charts in this case describe the steps discussed in section 2 fairly completely, but again minor points are not included. As soon as QV is entered, it calls a subroutine ADJERR (Fig. A-6) which changes the adaptive factor v_{α} discussed in section 5.2. At present a slightly larger than linear extrapolation formula is used to minimize the error in future numerical cycles. This is done only when there is a definite increasing trend in the error over the last three cycles; otherwise an average is used and if the error is oscillating between positive and negative values no correction is made at all.

At present the decrease of the time increment is based on how large the node voltage changes are rather than how large the circuit error is. This is a result of earlier indecision about which node voltage calculation criterion to use. Experience with the program has indicated the time interval change should rely more on the circuit error.

9.2 Sample Results

To demonstrate some of the properties of the IQ method, four circuits and their response will be presented here. The first, that of Fig. A-7, illustrates the effect of v_{α} on the circuit error. The maximum allowed error was set arbitrarily high so that the method would not decrease the size of the increments. When $v_{\alpha} = 0$, we see that the error in the initial two cycles after the application of the 10-volt step is very small but increases slowly, as discussed in section 5.2. The vast improvement by correctly changing v_{α} is noted, confirming the discussion of that section.

In the second example a tunnel diode monostable (Fig. A-8) is analyzed. The tunnel diode curve used is composed of three cubics for the tunneling, valley and diffusion regions of the diode which were found by a least-square

method of curve fitting. The same data was processed by the IQ method and by the second-order Runge-Kutta method, both of which gave the same response, agreeing within three millivolts at any given time. The circuit error in the IQ method was always less than one millivolt during the fast transients and even less at other times.

In the third example a tunnel diode pulse amplifier and waveform reshaper is considered. The tunnel diode on the input side had a peak current of two milliamperes and that on the output a five-milliamper peak. The two-milliamper tunnel diode triggers the five-milliamper diode which then supplies the output power. The effect of the coupling resistance R_c is observed in the two response diagrams. Since the average circuit error during the response was less than 0.5 millivolt, the waveforms can be expected to be fairly accurate.

As a final example, the reflections from an unbiased tunnel diode terminating a transmission line (Fig. A-10) are analyzed by the IQ method. The input pulse and the reflection appear in the v_s versus t plot. The initial negatively-reflected voltage occurs because of the low tunnel diode resistance in the tunneling region. After the peak is passed the resistance becomes negative, then very high, resulting in a positive voltage reflection coefficient. The final spike results from the capacitance discharging into the line. Since the sending end is correctly matched, it produces no reflections.

9.3 Efficiency

The program that is presently operative has been written in a manner so as to allow easy changes; efficiency was not a primary objective and consequently not much information can be gained by comparing the speed of computation of the present program with that of other methods. A more significant approach, an examination of the relative time spent in different parts of the program, indicates that the calculation of the branch currents and voltages in

QV by far uses the most time. This then leads to the conclusion that the time required to analyze a circuit will be proportional to the number of branches it has. To get an order of magnitude estimate of the speed of the IQ method on a computer we need therefore only consider the operations required in the branch loops of the program.

For ILLIAC II, for instance, it was found that about 20 additions, 30 multiplications and 50 access times will be required per branch calculation. Based on times of 3.5 μ sec, 6 μ sec, and 1.8 μ sec respectively for these three, this comes to a total of 350 μ sec per branch. Since branches with nonlinear elements will require more time, we can roughly say that the average time per branch calculation is 500 μ sec. Therefore a 20-branch circuit requiring 1000 steps for the solution should take about 10 seconds.

Two possible methods of increasing the speed of the IQ method should be mentioned. First, in most circuits there are many branches which are connected to ground, the reference node for the IQ method. Since these often contain only single elements such as resistances or capacitances, more simplified versions of the correction formula, equation 2.16, could be used for these special cases. Since sometimes as many as half of the branches will be connected to the reference node, this represents a significant increase in speed.

Second, for large circuits it is possible that one end is undergoing transients but the other is still in a steady state. Therefore the two parts of the circuit can be analyzed with different time increments. Although this will lead to problems in matching the time increments the result should be especially rewarding during the analysis of large transistor switching circuits.

10. CONCLUSIONS

At present not enough experience has been had with the IQ method to draw very definite conclusions about it. But, to summarize, we can restate some of its advantages and disadvantages. Among the advantages are the following:

- 1) An absolute error is available which the IQ method uses to make corrections.
- 2) An error correction mechanism is provided by the method for nonlinear elements, which eliminates the need for repetitive relaxation formulas.
- 3) The method is particularly suited for analyzing diode and transistor circuits since the provided error correction mechanism eliminates the need to integrate the transistor and diode equations separately and match the solutions with the rest of the circuit periodically. A second merit is that no further assumptions, aside from those used to get the Ebers and Moll equations, need to be made because of the convenient manner in which the relevant transistor quantities can be calculated.
- 4) The efficiency seems reasonable and the time required to analyze a circuit is linearly dependent on the number of branches in the circuit.
- 5) Programming is not too complicated since no matrices must be prepared and the initial conditions and transients can be calculated by the same routine.
- 6) The IQ method is very much directed toward giving the user insight into his circuit. The method deals with

quantities he can visualize and allows him to control more directly how the program handles his circuit.

The chief disadvantage is that the method will not handle all circuits with equal ease since it was developed for a circuit with a restricted topology. This will require some work from the user before he has his circuit in a form in which the method will handle it most efficiently. How serious these limitations can be is not yet known.

It is felt that at present the IQ method is still in too much of an untested state to allow a detailed comparison with other numerical methods for circuit analysis. But, considering the above advantages of the IQ method, it is also felt that it will certainly prove to be a useful tool and therefore deserves further analysis and refinement.

As a final note, it should be pointed out that the IQ method developed in this report is a consequence of the chosen topology and set of differences. It is possible that other incremental charge methods with better characteristics can be formulated by applying the same basic principles and deriving parallel formulas.

BIBLIOGRAPHY

- [1] Branin, F. H., Jr., "D-C and Transient Analysis of Networks Using a Digital Computer," IRE Int. Conv. Rec., Vol. 10, pt. 2, pp. 236-256, 1962.
- [2] Dewitt, D. and A. L. Rossoff, Transistor Electronics. McGraw-Hill Book Co., Inc., New York, New York, Chaps. 2, 3, 1957.
- [3] Domenico, R. J., "Simulation of Transistor Switching Circuits on the IBM 704," Trans. PGEC, EC-3, pp. 242-247, Dec., 1957.
- [4] Ebers, J. J. and J. L. Moll, "Large Signal Behavior of Junction Transistors," Proc. IRE, vol. 42, pp. 1761-1772, Dec., 1954.
- [5] Fosdick, L. D., "A Program for Calculating Node Voltages and Branch Currents in Circuits with Nonlinear Elements," Univ. of Ill., Dig. Comp. Lab. File No. 287, 1959.
- [6] Hamming, R. W., Numerical Methods for Scientists and Engineers, McGraw-Hill Book Co., Inc., New York, New York, Chap. 15, 1962.
- [7] Leichner, G. H., "General Tolerance Analysis Program (1206)," Univ. of Ill., Dig. Comp. Lab. File No. 255, 1958.
- [8] Poppelbaum, W. J. and N. E. Wiseman, "Circuit Design for the New Illinois Computer," Univ. of Ill., Dig. Comp. Lab. Report No. 90, 1959.

APPENDIX

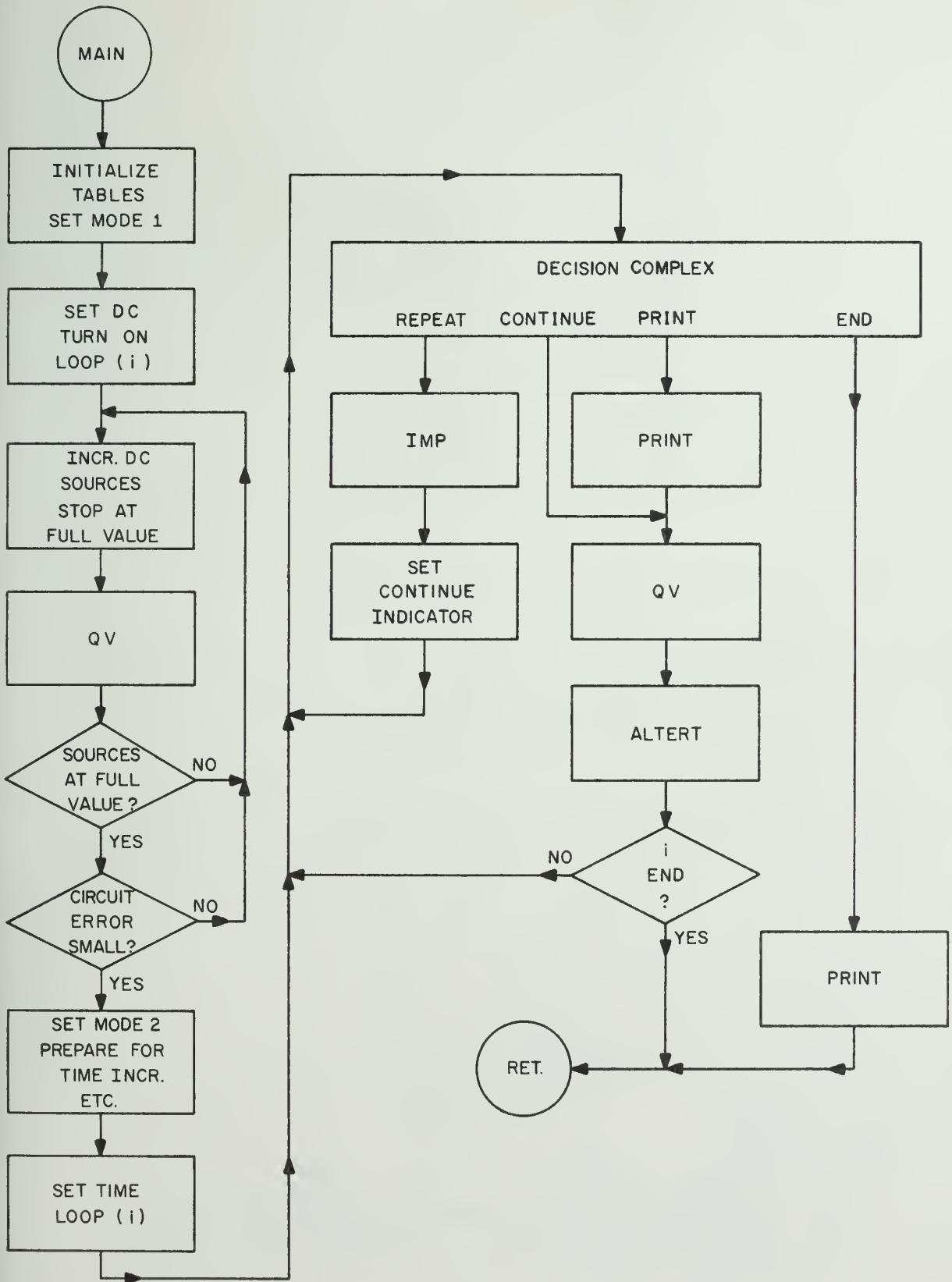


Figure A-1. Flow Chart for Main Routine.

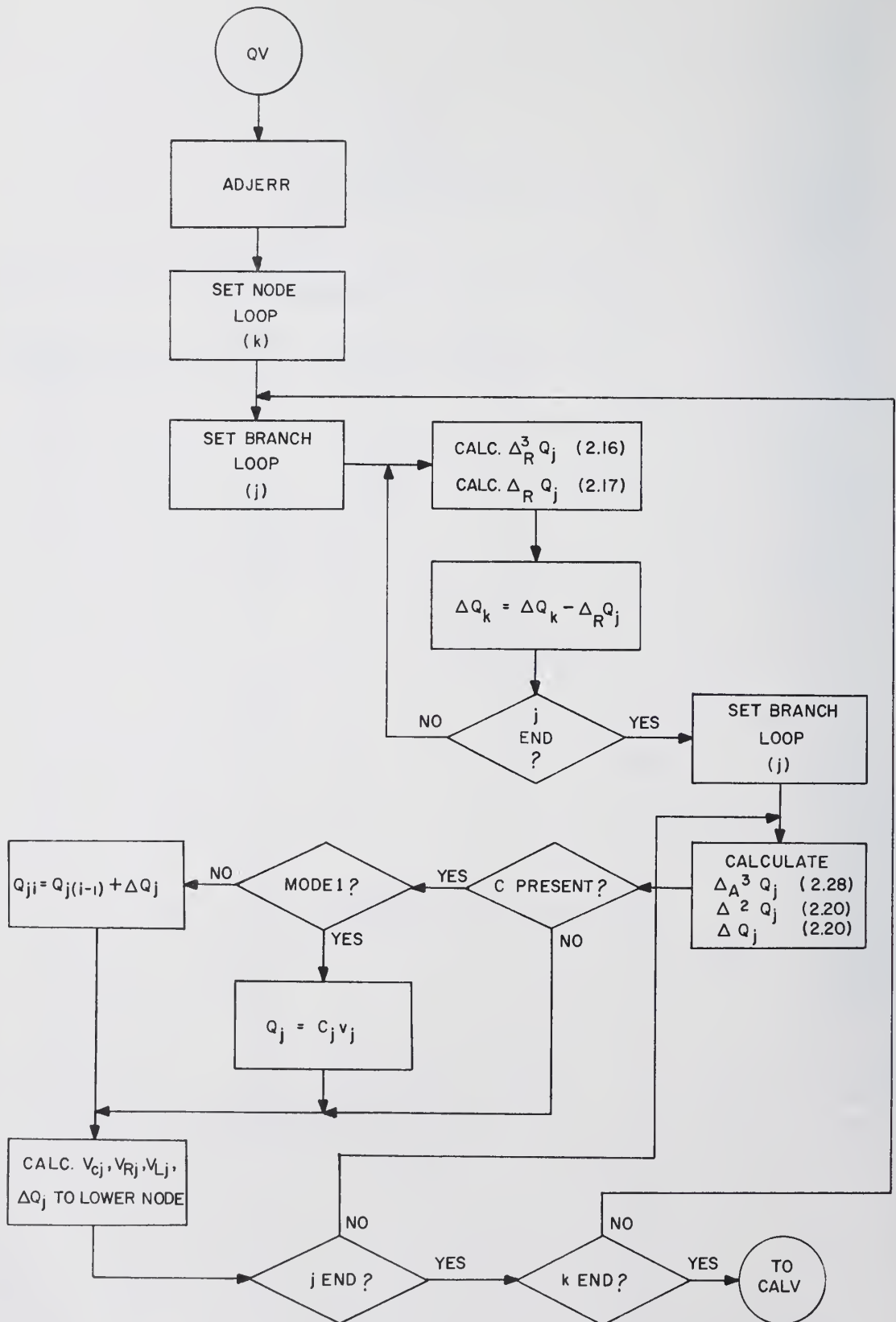


Figure A-2. Flow Chart for the Charge Distribution Cycle.

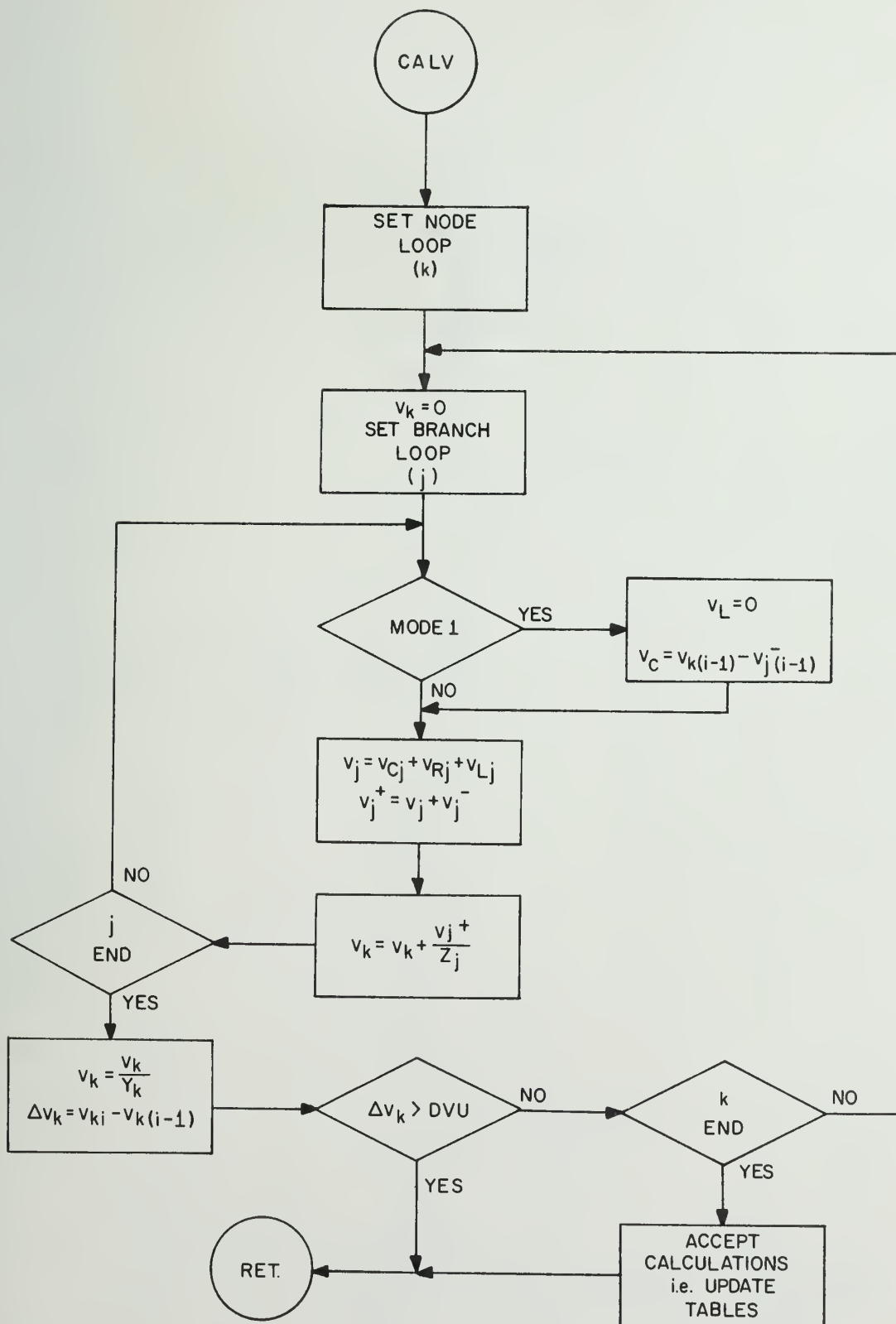


Figure A-3. Flow Chart for Node Voltage Calculation.

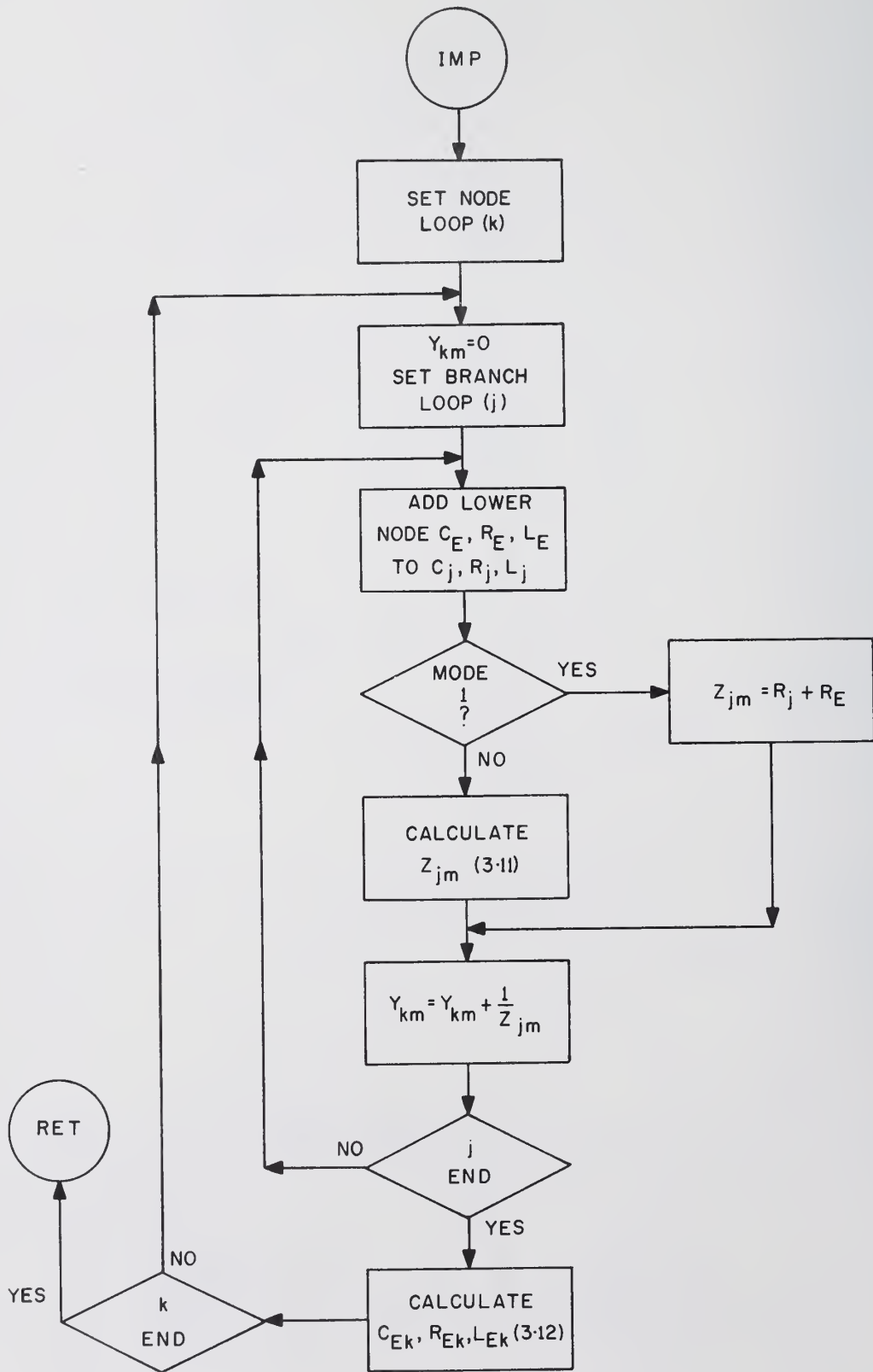


Figure A-4. Flow Chart for Impedance Factor Calculations.

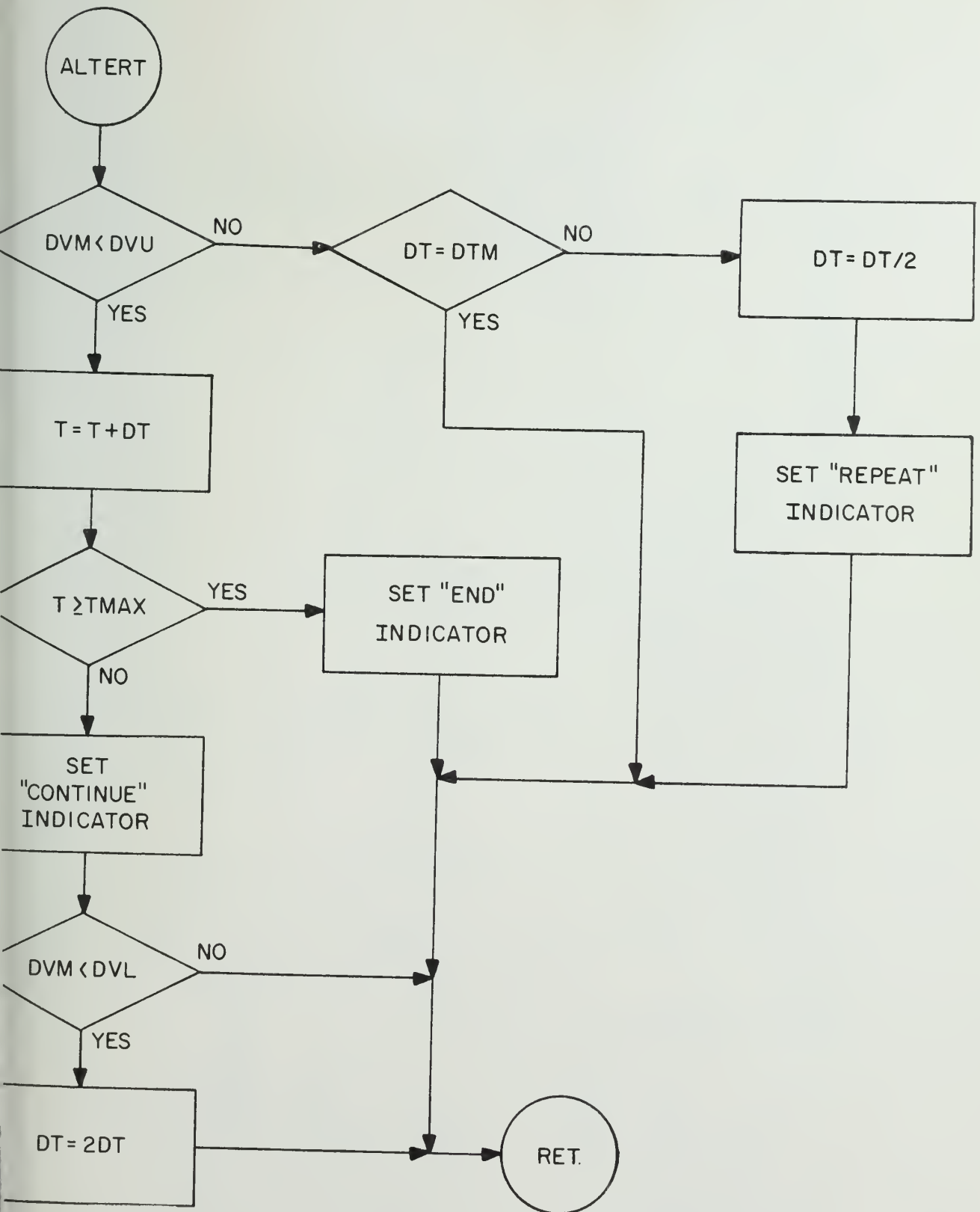


Figure A-5. Flow Chart for Δt Alteration Subroutine.

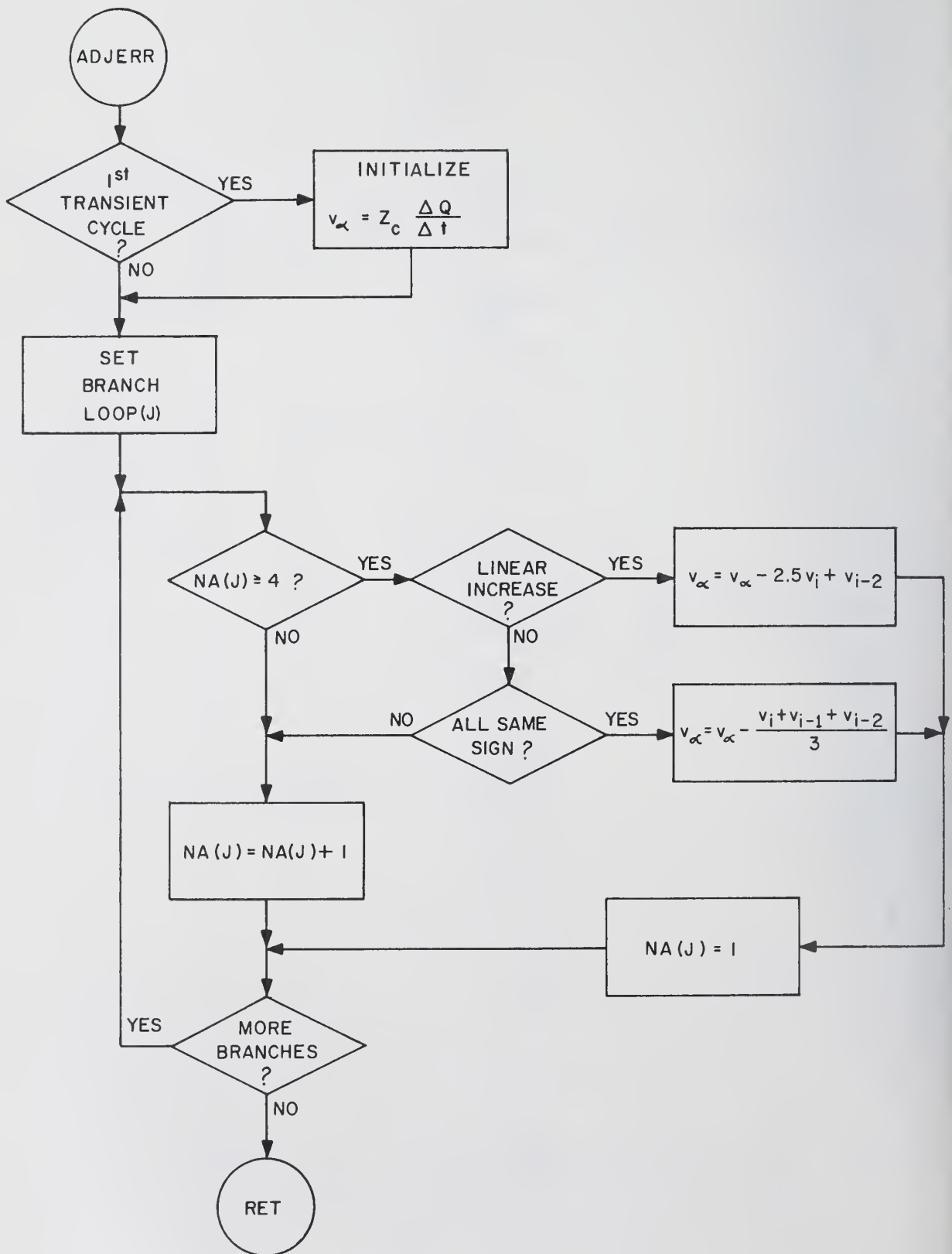


Figure A-6. Flow Chart for Adjusting v_{α} to the Error.

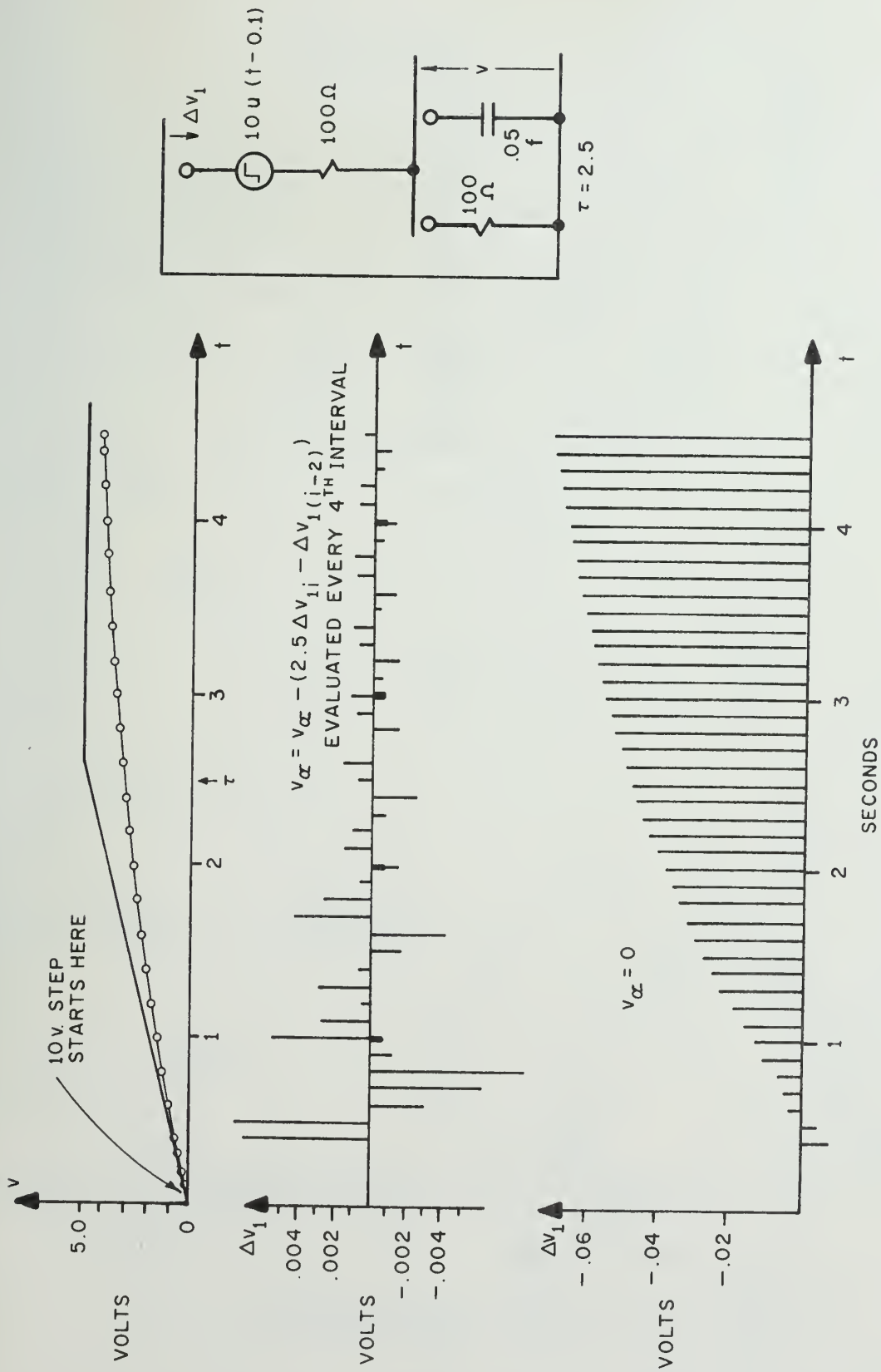
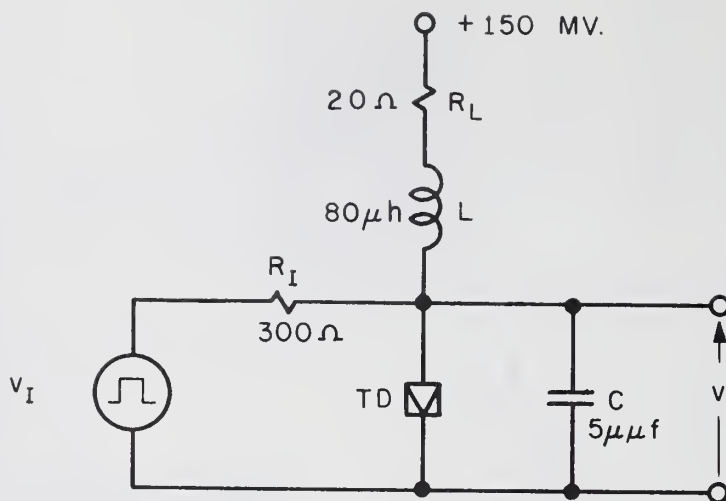
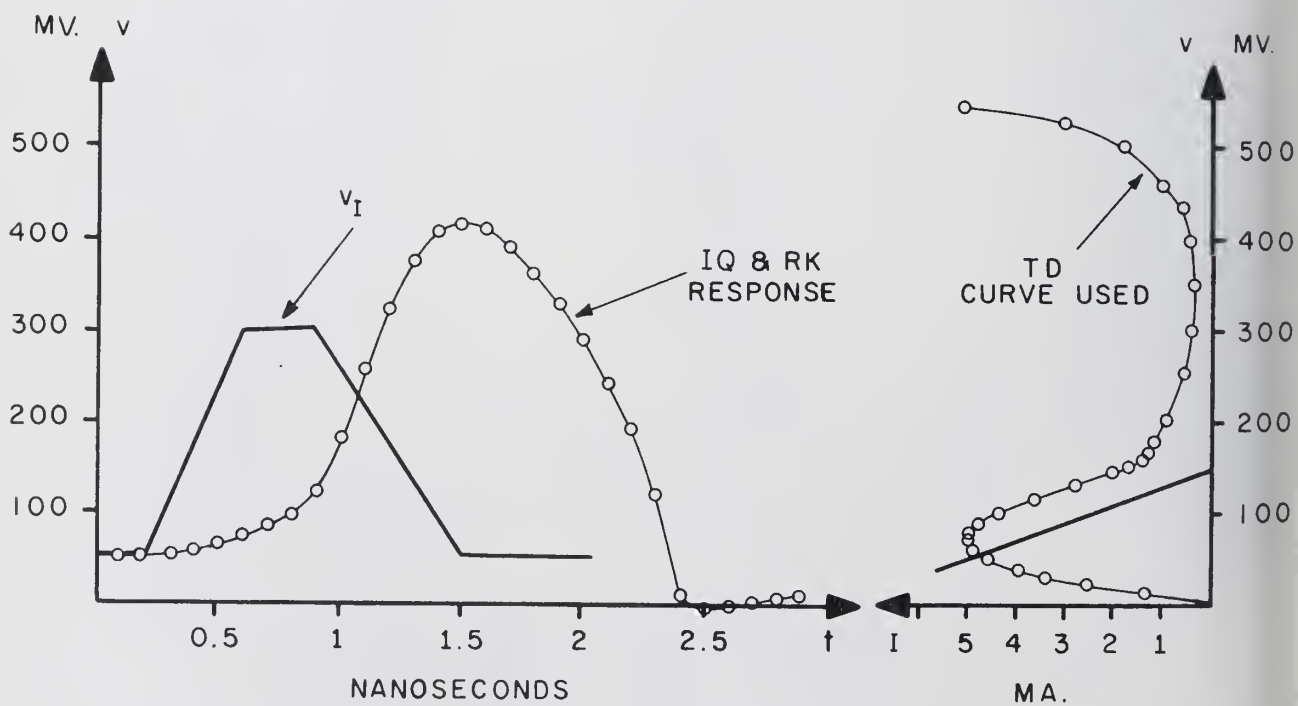


Figure A-7. RC Response and Effect of v_α on Circuit Error.

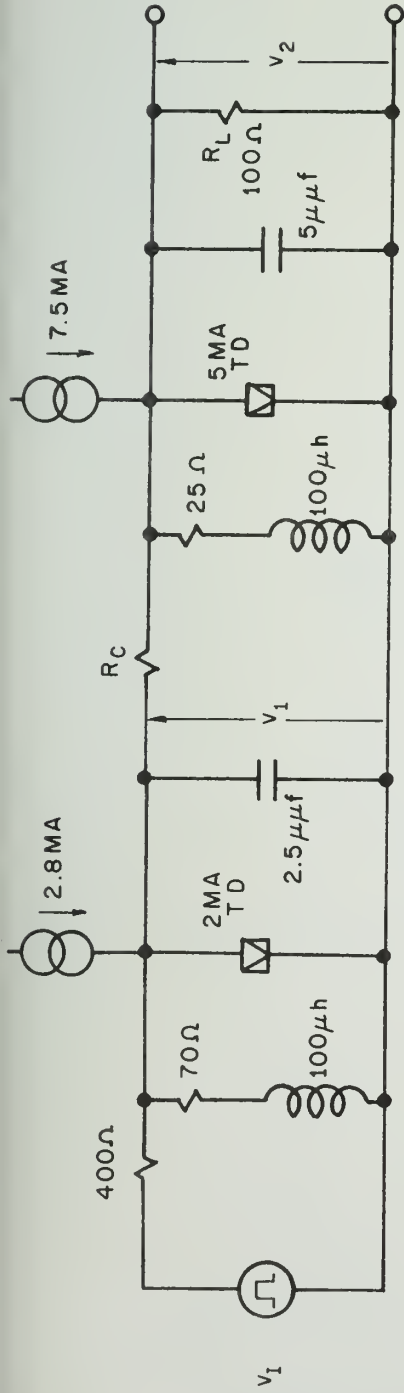


a) CIRCUIT

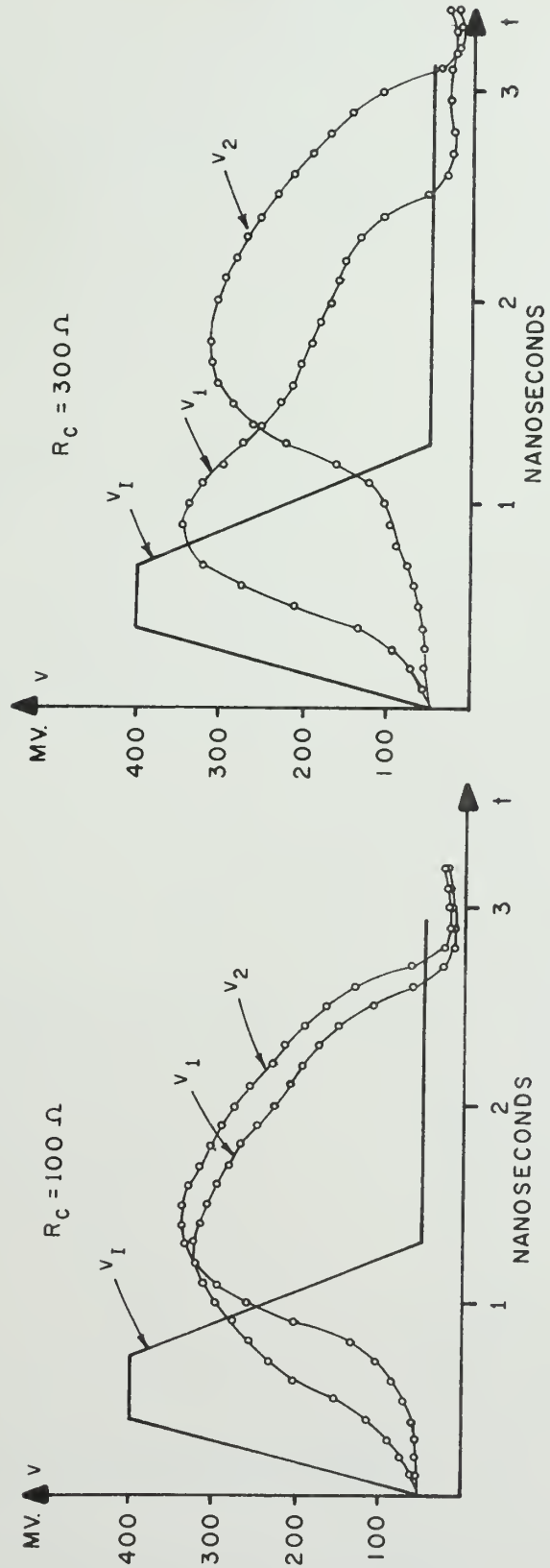


b) INPUT AND RESPONSE

Figure A-8. Tunnel Diode Monostable Response by the IQ Method and by the Second-Order Runge-Kutta Method.



a) CIRCUIT



b) RESPONSE

Figure A-9. Response of a Tunnel Diode Pulse Amplifier and Wave Reshaper.

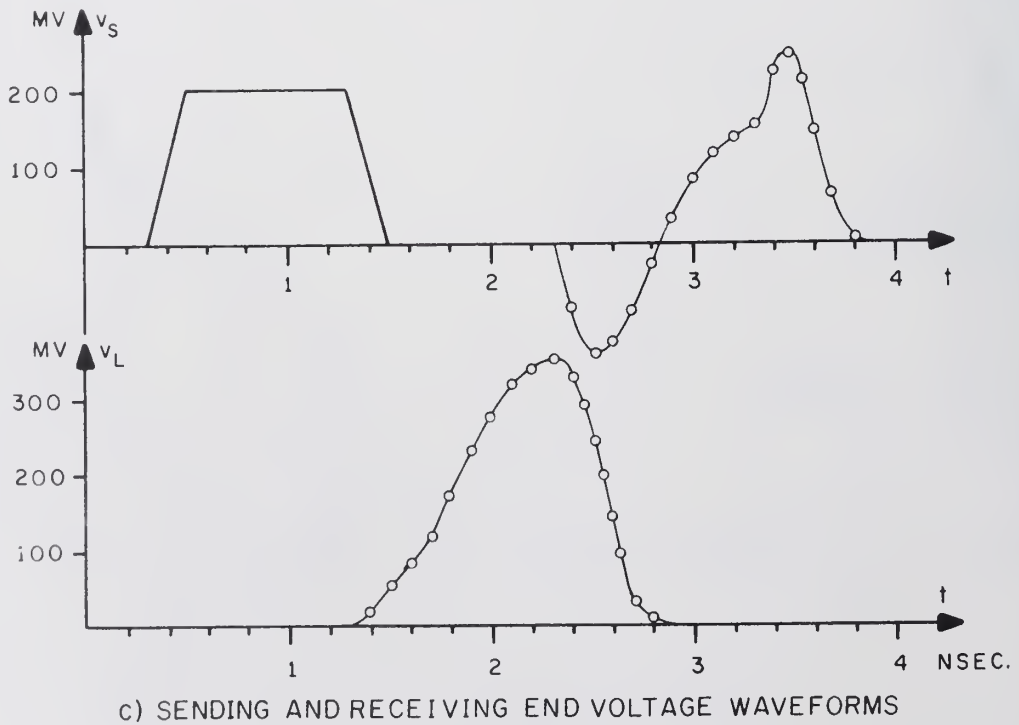
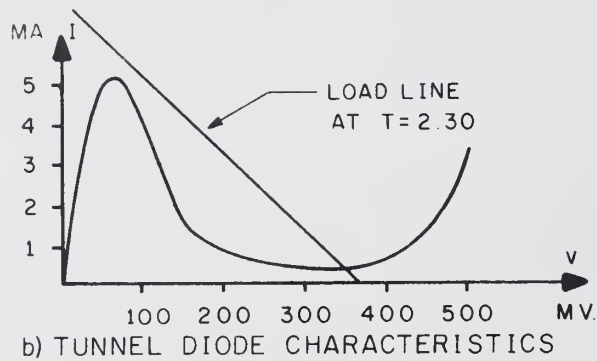
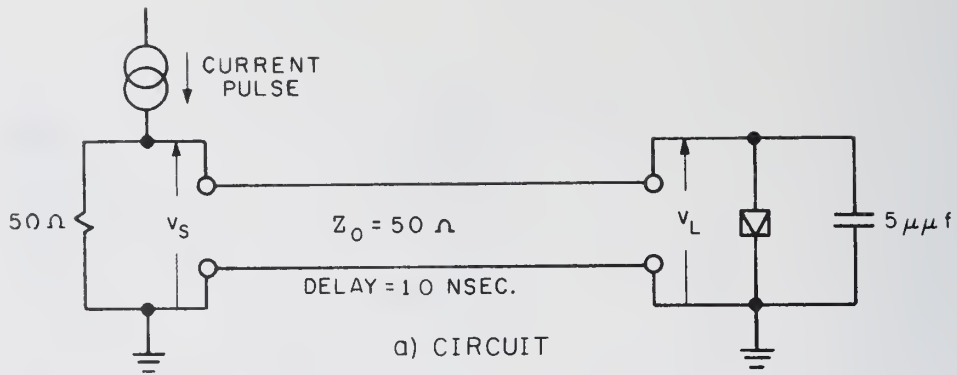


Figure A-10. Reflections from an Unbiased Tunnel Diode.



UNIVERSITY OF ILLINOIS-URBANA
510.84 IL6R no. C002 no.160-170(1964
Report /



3 0112 088398166